Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4112, 2.60 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate2017_int_base = 44.5
SPECrate2017_int_peak = 47.1

Hardware
CPU Name: Intel Xeon Silver 4112
Max MHz.: 3000
Nominal: 2600
Enabled: 8 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 8.25 MB I+D on chip per chip
Other: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)
Storage: 1 x 600 GB SAS HDD, 10K RPM
Other: None

Software
OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
Firmware: Version 3.2.1d released Sep-2017
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc: jemalloc memory allocator library
V5.0.1;
jemalloc: configured and built at default for
32bit (i686) and 64bit (x86_64) targets;
jemalloc: built with the RedHat Enterprise 7.4,
and the system compiler gcc 4.8.5;
jemalloc: sources available from jemalloc.net or releases
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Silver 4112, 2.60 GHz)

SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

Cisco Systems

2.60 GHz)

SPECrate2017_int_base = 44.5

SPECrate2017_int_peak = 47.1

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>16</td>
<td>785</td>
<td>32.4</td>
<td>780</td>
<td>32.6</td>
<td>783</td>
<td>32.5</td>
<td>16</td>
<td>622</td>
<td>40.9</td>
<td>622</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>16</td>
<td>562</td>
<td>40.3</td>
<td>562</td>
<td>40.3</td>
<td>562</td>
<td>40.3</td>
<td>16</td>
<td>480</td>
<td>47.2</td>
<td>481</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>16</td>
<td>457</td>
<td>56.6</td>
<td>459</td>
<td>56.4</td>
<td>464</td>
<td>55.7</td>
<td>16</td>
<td>456</td>
<td>56.7</td>
<td>466</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>16</td>
<td>745</td>
<td>28.2</td>
<td>743</td>
<td>28.2</td>
<td>746</td>
<td>28.1</td>
<td>16</td>
<td>743</td>
<td>28.3</td>
<td>744</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>16</td>
<td>344</td>
<td>49.2</td>
<td>339</td>
<td>49.8</td>
<td>342</td>
<td>49.4</td>
<td>16</td>
<td>295</td>
<td>57.2</td>
<td>296</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>16</td>
<td>329</td>
<td>85.2</td>
<td>327</td>
<td>85.7</td>
<td>328</td>
<td>85.3</td>
<td>16</td>
<td>318</td>
<td>88.2</td>
<td>316</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>16</td>
<td>489</td>
<td>77.5</td>
<td>489</td>
<td>77.5</td>
<td>489</td>
<td>77.5</td>
<td>16</td>
<td>488</td>
<td>37.6</td>
<td>489</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>16</td>
<td>759</td>
<td>34.9</td>
<td>760</td>
<td>34.9</td>
<td>761</td>
<td>34.8</td>
<td>16</td>
<td>754</td>
<td>35.2</td>
<td>753</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>16</td>
<td>511</td>
<td>82.1</td>
<td>512</td>
<td>81.9</td>
<td>512</td>
<td>81.9</td>
<td>16</td>
<td>511</td>
<td>82.0</td>
<td>511</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>16</td>
<td>537</td>
<td>32.2</td>
<td>538</td>
<td>32.1</td>
<td>537</td>
<td>32.2</td>
<td>16</td>
<td>537</td>
<td>32.2</td>
<td>537</td>
</tr>
</tbody>
</table>

SPECrate2017_int_base = 44.5

SPECrate2017_int_peak = 47.1

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise

(Continued on next page)
SPEC CPU2017 Integer Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4112, 2.60 GHz)

SPECrate2017_int_base = 44.5
SPECrate2017_int_peak = 47.1

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Nov-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

Power Performance Tuning set to OS
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-djj4 Wed Nov 22 00:41:26 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name: Intel(R) Xeon(R) Silver 4112 CPU @ 2.60GHz
2 "physical id"s (chips)
16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 4
siblings: 8
physical 0: cores 0 1 3 4
physical 1: cores 1 2 4 5

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 2
Core(s) per socket: 4
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4112 CPU @ 2.60GHz
Stepping: 4
CPU MHz: 799.874
CPU max MHz: 3000.0000
CPU min MHz: 800.0000
BogoMIPS: 5199.99
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 8448K

(Continued on next page)
SPEC CPU2017 Integer Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4112, 2.60 GHz)

SPECrate2017_int_base = 44.5
SPECrate2017_int_peak = 47.1

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

NUMA node0 CPU(s): 0-3, 8-11
NUMA node1 CPU(s): 4-7, 12-15
Flags:

fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpref eagerfpul pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb pln pts dtherm hwp
hw_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmx flexpriority ept vpid
fsqsbaset tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occup_llc

/platforminfo cache data
  cache size: 8448 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 8 9 10 11
node 0 size: 191913 MB
node 0 free: 188600 MB
node 1 cpus: 4 5 6 7 12 13 14 15
node 1 size: 193504 MB
node 1 free: 188792 MB
node distances:
  node 0 1
  0: 10 21
  1: 21 10

From /proc/meminfo
MemTotal: 394667604 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"

(Continued on next page)
**Platform Notes (Continued)**

```
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:
    Linux linux-djj4 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Dec 31 20:21
```

```
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 559G 128G 431G 23% /
```

**Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.**

```
BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
    24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400
```

(End of data from sysinfo program)

**Compiler Version Notes**

```
==============================================================================
 CC 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
    525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
```

```
==============================================================================
 CC 500.perlbench_r(peak) 502.gcc_r(peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
```

```
==============================================================================
 CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
        541.leela_r(base)
==============================================================================
icpc (ICC) 18.0.0 20170811
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4112, 2.60 GHz)

SPEC CPU2017 Integer Rate Result
Copyright 2017-2018 Standard Performance Evaluation Corporation

SPECrat2017_int_base = 44.5
SPECrat2017_int_peak = 47.1

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

______________________________________________________________________________
CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
541.leela_r(peak)
______________________________________________________________________________
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
______________________________________________________________________________
FC 548.exchange2_r(base, peak)
______________________________________________________________________________
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
______________________________________________________________________________

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4112, 2.60 GHz)

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>SPECrate2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>44.5</td>
<td>47.1</td>
</tr>
</tbody>
</table>

**Base Optimization Flags**

C benchmarks:
- `-Wl,-z,muldefs`  
- `-xCORE-AVX512`  
- `-ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=3`  
- `-L/usr/local/je5.0.1-64/lib`  
- `-ljemalloc`

C++ benchmarks:
- `-Wl,-z,muldefs`  
- `-xCORE-AVX512`  
- `-ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=3`  
- `-L/usr/local/je5.0.1-64/lib`  
- `-ljemalloc`

Fortran benchmarks:
- `-Wl,-z,muldefs`  
- `-xCORE-AVX512`  
- `-ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=3`  
- `-nostandard-realloc-lhs`  
- `-align array32byte`  
- `-L/usr/local/je5.0.1-64/lib`  
- `-ljemalloc`

**Base Other Flags**

C benchmarks:
- `-m64 -std=c11`

C++ benchmarks:
- `-m64`

Fortran benchmarks:
- `-m64`

**Peak Compiler Invocation**

C benchmarks:
- `icc`

C++ benchmarks:
- `icpc`

Fortran benchmarks:
- `ifort`

**Peak Portability Flags**

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-D_FILE_OFFSET_BITS=64`

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4112, 2.60 GHz)

SPECrate2017_int_base = 44.5
SPECrate2017_int_peak = 47.1

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Portability Flags (Continued)

505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib
-ljemalloc

502.gcc_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib
-ljemalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib
-ljemalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:
520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-64/lib -ljemalloc

523.xalancbmk_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

(Continued on next page)
**SPEC CPU2017 Integer Rate Result**

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Silver 4112, 2.60 GHz)

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>44.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_int_peak</td>
<td>47.1</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Nov-2017

**Tested by:** Cisco Systems  
**Hardware Availability:** Aug-2017

**Tested with SPEC CPU2017 v1.0.2 on 2017-11-22 00:41:25-0500.**

**Software Availability:** Sep-2017

---

### Peak Optimization Flags (Continued)

- 531.deepsjeng_r: Same as 520.omnetpp_r
- 541.leela_r: Same as 520.omnetpp_r

**Fortran benchmarks:**

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

### Peak Other Flags

**C benchmarks (except as noted below):**

- `-m64 -std=c11`

- 502.gcc_r: `-m32 -std=c11`

**C++ benchmarks (except as noted below):**

- `-m64`

- 523.xalancbmk_r: `-m32`

**Fortran benchmarks:**

- `-m64`

---

The flags files that were used to format this result can be browsed at:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

---

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2017-11-22 00:41:25-0500.


Originally published on 2017-12-26.