# SPEC® CPU2017 Integer Rate Result

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4112, 2.60 GHz)

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>SPECrate2017_int_peak</th>
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<tr>
<td>44.0</td>
<td>46.9</td>
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</tbody>
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**CPU2017 License:** 9019  
**Test Date:** Dec-2017  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Aug-2017  
**Tested by:** Cisco Systems  
**Software Availability:** Sep-2017

### Hardware

| CPU Name | Intel Xeon Silver 4112  
| Max MHz | 3000  
| Nominal | 2600  
| Enabled | 8 cores, 2 chips, 2 threads/core  
| Orderable | 1,2 Chips  
| Cache L1 | 32 KB I + 32 KB D on chip per core  
| L2 | 1 MB I+D on chip per core  
| L3 | 8.25 MB I+D on chip per chip  
| Other | None  
| Memory | 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)  
| Storage | 1 x 600 GB SAS HDD, 10K RPM  
| Other | None  

### Software

| OS | SUSE Linux Enterprise Server 12 SP2 (x86_64)  
| Compiler | C/C++: Version 18.0.0.128 of Intel C/C++  
| Compiler for Linux |  
| Fortran | Version 18.0.0.128 of Intel Fortran  
| Compiler for Linux |  
| Parallel | No  
| Firmware | Version 3.1.1d released Sep-2017  
| File System | xfs  
| System State | Run level 3 (multi-user)  
| Base Pointers | 64-bit  
| Peak Pointers | 32/64-bit  
| Other |  

### Copies

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
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<tbody>
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<td>40.6</td>
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<tr>
<td>39.7</td>
<td>52.5</td>
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<tr>
<td>54.2</td>
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<td>32.1</td>
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</tbody>
</table>

SPECrate2017_int_base = 44.0  SPECrate2017_int_peak = 46.9

Results Table

Submit Notes
The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise

(Continued on next page)
Platform Notes (Continued)

Power Performance Tuning set to OS
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-a0tk Tue Dec 5 19:17:03 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Silver 4112 CPU @ 2.60GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 4
  siblings : 8
  physical 0: cores 1 2 4 5
  physical 1: cores 0 1 3 4

From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 16
  On-line CPU(s) list: 0-15
  Thread(s) per core: 2
  Core(s) per socket: 4
  Socket(s): 2
  NUMA node(s): 2
  Vendor ID: GenuineIntel
  CPU family: 6
  Model: 85
  Model name: Intel(R) Xeon(R) Silver 4112 CPU @ 2.60GHz
  Stepping: 4
  CPU MHz: 2824.338
  CPU max MHz: 3000.0000
  CPU min MHz: 800.0000
  BogoMIPS: 5187.84
  Virtualization: VT-x
  L1d cache: 32K
  L1i cache: 32K
  L2 cache: 1024K
  L3 cache: 8448K

(Continued on next page)
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---

### Platform Notes (Continued)

**NUMA node0 CPU(s):**  
0-3, 8-11

**NUMA node1 CPU(s):**  
4-7, 12-15

**Flags:**
```
fpu vme de pse tsc msr pae mca cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl mca nobreak ring87
xt86d oval ibs lahf_lm abm 3nowprefetch ida arat epb pln pts dtherm hwp
```

**/proc/cpuinfo cache data**
```
cache size : 8448 KB
```

---

From `numactl --hardware`
```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```
```
available: 2 nodes (0-1)  
node 0 cpus: 0 1 2 3 8 9 10 11  
node 0 size: 192090 MB  
node 0 free: 187852 MB  
node 1 cpus: 4 5 6 7 12 13 14 15  
node 1 size: 193518 MB  
node 1 free: 190282 MB  
node distances:
node  0 1
0: 10 21  
1: 21 10
```

From `/proc/meminfo`
```
MemTotal: 394863492 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB
```

From `/usr/bin/lsb_release -d`
```
SUSE Linux Enterprise Server 12 SP2
```

From `/etc/*release* /etc/*version*`
```
SuSE-release:
```
```
SUSE Linux Enterprise Server 12 (x86_64)  
VERSION = 12  
PATCHLEVEL = 2  
```

# This file is deprecated and will be removed in a future service pack or release.  
# Please check /etc/os-release for details about this release.  

os-release:
```
NAME="SLES"
```
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**SPECrat02017_int_base = 44.0**  
**SPECrat02017_int_peak = 46.9**

---

**Platform Notes (Continued)**

```
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

uname -a:
```
Linux linux-a0tk 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Dec 5 04:58
```

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda7 xfs 416G 119G 298G 29% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
Memory:
```
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400
```

(End of data from sysinfo program)

---

**Compiler Version Notes**

```
---
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
  525.x264_r(base, peak) 557.xz_r(base, peak)
---
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
---
---
CC  500.perlbench_r(peak) 502.gcc_r(peak)
---
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
---
---
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
---
```

(Continued on next page)
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### Compiler Version Notes (Continued)

```
541.leela_r(base)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
541.leela_r(peak)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
FC 548.exchange2_r(base, peak)

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
```

### Base Compiler Invocation

**C benchmarks:**
- icc

**C++ benchmarks:**
- icpc

**Fortran benchmarks:**
- ifort

### Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
```

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Base Portability Flags (Continued)
557.xz_r: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Base Other Flags
C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

Fortran benchmarks:
-m64

Peak Compiler Invocation
C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort
## Peak Portability Flags

<table>
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<tr>
<th>Benchmark</th>
<th>Flags</th>
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<tbody>
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<td>500.perlbench_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>-D_FILE_OFFSET_BITS=64</td>
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<tr>
<td>505.mcf_r</td>
<td>-DSPEC_LP64</td>
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<tr>
<td>520.omnetpp_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
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<td>-DSPEC_LP64</td>
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<tr>
<td>557.xz_r</td>
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## Peak Optimization Flags

### C benchmarks:

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<tr>
<td>500.perlbench_r</td>
<td>-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>-L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>-l/usr/local/je5.0.1-32/lib -ljemalloc</td>
</tr>
</tbody>
</table>

### C++ benchmarks:

<table>
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<tr>
<td>520.omnetpp_r</td>
<td>-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>-L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32</td>
</tr>
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### Peak Optimization Flags (Continued)

523.xalancbmk_r (continued):

- `-L/usr/local/je5.0.1-32/lib -ljemalloc`

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

ForTRAN benchmarks:

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-gopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

### Peak Other Flags

C benchmarks (except as noted below):

- `-m64 -std=c11`

502.gcc_r: `-m32 -std=c11`

C++ benchmarks (except as noted below):

- `-m64`

523.xalancbmk_r: `-m32`

ForTRAN benchmarks:

- `-m64`

The flags files that were used to format this result can be browsed at:

- [Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)
- [Cisco-Platform-Settings-V1.2-revH.html](http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html)

You can also download the XML flags sources by saving the following links:

- [Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)
- [Cisco-Platform-Settings-V1.2-revH.xml](http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml)

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