## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
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<tr>
<td></td>
<td>54.5</td>
<td>55.4</td>
</tr>
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</table>

<table>
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<tr>
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<th>9019</th>
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<td>Cisco Systems</td>
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<td>Cisco Systems</td>
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<tr>
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### Threads

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<td>34.2</td>
<td>38.2</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>34.1</td>
<td>34.1</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>51.7</td>
<td>55.8</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>29.3</td>
<td>29.3</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>45.7</td>
<td>47.0</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>33.5</td>
<td>35.6</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>57.1</td>
<td>57.0</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>58.3</td>
<td>58.3</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>59.1</td>
<td>59.1</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 5122
- **Max MHz:** 3700
- **Nominal:** 3600
- **Enabled:** 8 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 16.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 1 TB SAS HDD, 7.2K RPM
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.2.1d released Jul-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --
## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems
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---

## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Seconds</th>
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<tr>
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<tr>
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<td>627.cam4_s</td>
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<td>29.2</td>
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<td>29.3</td>
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<td>29.3</td>
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<td>628.pop2_s</td>
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<td>260</td>
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<td>259</td>
<td>45.8</td>
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<td>47.2</td>
<td>253</td>
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<td>431</td>
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<td>426</td>
<td>33.8</td>
<td>431</td>
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<td>307</td>
<td>57.0</td>
<td>306</td>
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<td>56.2</td>
<td>267</td>
<td>59.1</td>
<td>260</td>
<td>60.5</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

## Platform Notes

BIOS Settings:

- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS
- SNC set to Disabled
- IMC Interleaving set to Auto
- Patrol Scrub set to Disabled
- Sysinfo program /home/cpu2017/bin/sysinfo
- Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

(Continued on next page)
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Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

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Platform Notes (Continued)

running on linux-djj4 Sun Dec 10 12:08:54 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
  2 "physical id"s (chips)
  8 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings  : 4
  physical 0: cores 1 2 5 11
  physical 1: cores 1 2 5 11
```

From lscpu:
```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                8
On-line CPU(s) list:   0-7
Thread(s) per core:    1
Core(s) per socket:    4
Socket(s):             2
NUMA node(s):          2
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
Stepping:              4
CPU MHz:               1530.137
CPU max MHz:           3700.0000
CPU min MHz:           1200.0000
BogoMIPS:              7200.02
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              16896K
NUMA node0 CPU(s):     0-3
NUMA node1 CPU(s):     4-7
```

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
       pat pse36 cplflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
       lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
       aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg

(Continued on next page)
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Platform Notes (Continued)

fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmvi flexpriority ept vpid
fsgsbase tsc_adjust bm1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavек
xgetbv1 cqm_l1c cqm_occup_l1c

/proc/cpuinfo cache data
cache size: 16896 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
nod е 0 cpus: 0 1 2 3
node 0 size: 191913 MB
node 0 free: 187891 MB
node 1 cpus: 4 5 6 7
node 1 size: 193504 MB
node 1 free: 189618 MB
node distances:
nod e 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 394667636 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-djj4 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

SPEC CPU®2017 Floating Point Speed Result

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Cisco Systems

SPECspeed®2017_fp_base = 54.5
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Platform Notes (Continued)

x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 3 01:01

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 559G 127G 432G 23% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
| 644.nab_s(base, peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

 ICC, C, Fortran | 607.cactuBSSN_s(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Fortran | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

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Compiler Version Notes (Continued)

==============================================================================
Fortran, C | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
| 628.pop2_s(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
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### Base Optimization Flags

- **C benchmarks:**
  - `xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
  - `-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP`

- **Fortran benchmarks:**
  - `-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
  - `-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp`
  - `-nostandard-realloc-lhs -align array32byte`

- **Benchmarks using both Fortran and C:**
  - `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
  - `-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP`
  - `-nostandard-realloc-lhs -align array32byte`

- **Benchmarks using Fortran, C, and C++:**
  - `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
  - `-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP`
  - `-nostandard-realloc-lhs -align array32byte`

### Base Other Flags

- **C benchmarks:**
  - `-m64 -std=c11`

- **Fortran benchmarks:**
  - `-m64`

- **Benchmarks using both Fortran and C:**
  - `-m64 -std=c11`

- **Benchmarks using Fortran, C, and C++:**
  - `-m64 -std=c11`

### Peak Compiler Invocation

- **C benchmarks:**
  - `icc`

- **Fortran benchmarks:**
  - `ifort`
## Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
```
ifort icc
```

Benchmarks using Fortran, C, and C++:
```
icpc icc ifort
```

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

**C benchmarks:**
```
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s
```

**Fortran benchmarks:**
```
-wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:
```
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte
```

(Continued on next page)
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Peak Optimization Flags (Continued)

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch
-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte

Peak Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-12-10 12:08:54-0500.
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