## SPEC®CPU2017 Integer Speed Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Gold 6128, 3.40 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.45</td>
<td>8.72</td>
</tr>
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</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Dec-2017  
**Hardware Availability:** Aug-2017

<table>
<thead>
<tr>
<th>Threads</th>
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<tr>
<td>600.perlbench_s</td>
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<td>602.gcc_s</td>
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<td>605.mcf_s</td>
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<tr>
<td>620.omnetpp_s</td>
<td>12</td>
<td>5.85</td>
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<tr>
<td>623.xalancbmk_s</td>
<td>12</td>
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<tr>
<td>625.x264_s</td>
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<td>4.34</td>
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<td>631.deepsjeng_s</td>
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<td>641.leela_s</td>
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<td>648.exchange2_s</td>
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<tr>
<td>657.xz_s</td>
<td>12</td>
<td>4.36</td>
</tr>
</tbody>
</table>

**Software**

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.2.1d released Jul-2017
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc: jemalloc memory allocator library V5.0.1; jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets; jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5; jemalloc: sources available from jemalloc.net or releases
- **Power Management:** --

**Hardware**

- **CPU Name:** Intel Xeon Gold 6128  
  - **Max MHz:** 3700  
  - **Nominal:** 3400  
  - **Enabled:** 12 cores, 2 chips  
  - **Orderable:** 1.2 Chips  
  - **Cache L1:** 32 KB I + 32 KB D on chip per core  
  - **L2:** 1 MB I+D on chip per core  
  - **L3:** 19.25 MB I+D on chip per chip  
  - **Other:** None  
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)  
- **Storage:** 1 x 1 TB SAS HDD, 7.2K RPM  
- **Other:** None
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6128, 3.40 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Results Table

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<tr>
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<th>Threads</th>
<th>Seconds</th>
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<td>15.4</td>
<td>401</td>
<td>15.4</td>
<td>401</td>
<td>15.4</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "'/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

(Continued on next page)
# Platform Notes (Continued)

running on linux-djj4 Tue Dec  5 06:11:04 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
  2 "physical id"s (chips)
  12 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 6
siblings : 6
physical 0: cores 0 6 9 10 11 13
physical 1: cores 0 6 9 10 11 13
```

From lscpu:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                12
On-line CPU(s) list:   0-11
Thread(s) per core:    1
Core(s) per socket:    6
Socket(s):             2
NUMA node(s):          2
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
Stepping:              4
CPU MHz:               1409.842
CPU max MHz:           3700.0000
CPU min MHz:           1200.0000
BogoMIPS:              6800.00
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              19712K
NUMA node0 CPU(s):     0-5
NUMA node1 CPU(s):     6-11
```

Flags: fpu vme move pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 cgflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6128, 3.40 GHz)

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**Platform Notes (Continued)**

fma cx16 xtpr pdcm pcid dca ssse4_1 ssse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmvi flexpriority ept vpid
fsqsbasc tsc_adjust bni1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavc
xgetbv1 cqm_llc cqm_occu_up llc

/proc/cpuinfo cache data
cache size: 19712 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5
node 0 size: 191913 MB
node 0 free: 191317 MB
node 1 cpus: 6 7 8 9 10 11
node 1 size: 193504 MB
node 1 free: 192872 MB
node distances:
node 0 1
 0: 10 21
 1: 21 10

From /proc/meminfo
MemTotal: 394667620 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-djj4 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)

(Continued on next page)
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SPECspeed®2017_int_base = 8.45
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Platform Notes (Continued)

x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 3 21:08

SPEC is set to: /home/cpu2017
Filesysten Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 559G 133G 427G 24% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
C++ | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
==============================================================================
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 648.exchange2_s(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
### Cisco Systems
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### Base Compiler Invocation
- **C benchmarks:** 
  icc
- **C++ benchmarks:** 
  icpc
- **Fortran benchmarks:** 
  ifort

### Base Portability Flags
- `600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `602.gcc_s: -DSPEC_LP64`
- `605.mcf_s: -DSPEC_LP64`
- `620.omnetpp_s: -DSPEC_LP64`
- `623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX`
- `625.x264_s: -DSPEC_LP64`
- `631.deepsjeng_s: -DSPEC_LP64`
- `641.leela_s: -DSPEC_LP64`
- `648.exchange2_s: -DSPEC_LP64`
- `657.xz_s: -DSPEC_LP64`

### Base Optimization Flags
- **C benchmarks:** 
  `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
  `-qopt-mem-layout-trans=3 -gopenmp -DSPEC_OPENMP`  
  `-L/usr/local/je5.0.1-64/lib -ljemalloc`
- **C++ benchmarks:** 
  `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
  `-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc`
- **Fortran benchmarks:** 
  `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
  `-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`  
  `-L/usr/local/je5.0.1-64/lib -ljemalloc`
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### Base Other Flags
- C benchmarks:
  -m64  -std=c11
- C++ benchmarks:
  -m64
- Fortran benchmarks:
  -m64

### Peak Compiler Invocation
- C benchmarks:
  icc
- C++ benchmarks:
  icpc
- Fortran benchmarks:
  ifort

### Peak Portability Flags
- 600.perlbmk_s: -DSPEC_LP64 -DSPEC_LINUX_X64
- 602.gcc_s: -DSPEC_LP64
- 605.mcf_s: -DSPEC_LP64
- 620.omnetpp_s: -DSPEC_LP64
- 623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
- 625.x264_s: -DSPEC_LP64
- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64
- 657.xz_s: -DSPEC_LP64

### Peak Optimization Flags
- C benchmarks:
  600.perlbmk_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
  -xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
  -no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp

(Continued on next page)
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Peak Optimization Flags (Continued)

600.perlbench_s (continued):
-DSPEC_OPENMP -fno-strict-overflow
-\(\text{L/\text{usr/local/je5.0.1-64/lib -ljemalloc}}\)

602.gcc_s: -\(\text{Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2}\)
-\(\text{xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3}\)
-\(\text{no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp}\)
-\(\text{DSPEC_OPENMP -L/\text{usr/local/je5.0.1-64/lib -ljemalloc}}\)

605.mcf_s: -\(\text{Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo}\)
-\(\text{xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3}\)
-\(\text{DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP}\)
-\(\text{L/\text{usr/local/je5.0.1-64/lib -ljemalloc}}\)

625.x264_s: -\(\text{Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div}\)
-\(\text{qopt-mem-layout-trans=3 -gopenmp -DSPEC_OPENMP}\)
-\(\text{L/\text{usr/local/je5.0.1-64/lib -ljemalloc}}\)

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: -\(\text{Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo}\)
-\(\text{xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3}\)
-\(\text{DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP}\)
-\(\text{L/\text{usr/local/je5.0.1-64/lib -ljemalloc}}\)

623.xalancbmk_s: -\(\text{L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32}\)
-\(\text{Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo}\)
-\(\text{xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3}\)
-\(\text{DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP}\)
-\(\text{L/\text{usr/local/je5.0.1-32/lib -ljemalloc}}\)

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:

-\(\text{Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div}\)
-\(\text{qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte}\)
-\(\text{L/\text{usr/local/je5.0.1-64/lib -ljemalloc}}\)
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</table>

**Peak Other Flags**

C benchmarks:
- -m64 -std=c11

C++ benchmarks (except as noted below):
- -m64

623.xalancbmk_s: -m32

Fortran benchmarks:
- -m64

The flags files that were used to format this result can be browsed at:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-12-05 06:11:03-0500.
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