Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

SPECrate®2017_fp_base = 69.7
SPECrate®2017_fp_peak = 71.9

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<th>Test Sponsor:</th>
<th>Cisco Systems</th>
<th>CPU2017 License:</th>
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<td>Test Date:</td>
<td>Dec-2017</td>
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<td>Aug-2017</td>
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<td></td>
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<td>Software Availability:</td>
<td>Sep-2017</td>
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</table>

### Hardware

**CPU Name:** Intel Xeon Gold 5122  
**Max MHz:** 3700  
**Nominal:** 3600  
**Enabled:** 8 cores, 2 chips, 2 threads/core  
**Orderable:** 1.2 Chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 16.5 MB I+D on chip per core  
**Other:** None  
**Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)  
**Storage:** 1 x 1 TB SAS HDD, 7.2K RPM  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)  
4.4.21-69-default  
**Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux  
**Parallel:** No  
**Firmware:** Version 3.2.1d released Jul-2017  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 64-bit  
**Other:** None  
**Power Management:** --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/jre5.0.1-32:/home/cpu2017/jre5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
 sync; echo 3> /proc/sys/vm/drop_caches
## Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Enabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS
- SNC set to Enabled
- IMC Interleaving set to 1-way Interleave
- Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-djj4 Fri Dec 8 18:33:29 2017

SUT (System Under Test) info as seen by some common utilities. For more information on this section, see [https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
- 2 "physical id"s (chips)
- 16 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores: 4
  - siblings: 8
  - physical 0: cores 1 2 5 11
  - physical 1: cores 1 2 5 11

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 16
- On-line CPU(s) list: 0-15
- Thread(s) per core: 2
- Core(s) per socket: 4
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
- Stepping: 4
- CPU MHz: 3553.669
- CPU max MHz: 3700.0000
- CPU min MHz: 1200.0000
- BogoMIPS: 7200.06
- Virtualization: VT-x
- L1d cache: 32K

(Continued on next page)
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

SPEC®2017_FP Peak = 71.9
SPEC®2017_FP Base = 69.7

CPU2017 License: 9019
Test Date: Dec-2017
Test Sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Sep-2017

Platform Notes (Continued)

L1i cache: 32K
L2 cache: 1024K
L3 cache: 16896K
NUMA node0 CPU(s): 0-3, 8-11
NUMA node1 CPU(s): 4-7, 12-15
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acp lmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtcsl64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb pns dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmvi crypto cpuid

From /proc/cpuinfo cache data
    cache size : 16896 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 8 9 10 11
    node 0 size: 191913 MB
    node 0 free: 191229 MB
    node 1 cpus: 4 5 6 7 12 13 14 15
    node 1 size: 193504 MB
    node 1 free: 192859 MB
    node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
    MemTotal: 394667604 kB
    HugePages_Total: 0
    Hugepagesize: 2048 KB

From /etc/*release*/os-release*
    SUSE-release:
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
    NAME="SLES"
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 69.7
SPECrate®2017_fp_peak = 71.9

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-djj4 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 1 02:40

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 559G 126G 434G 23% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |
| icc (ICC) 18.0.0 20170811 |
| Copyright (C) 1985-2017 Intel Corporation. All rights reserved. |

==============================================================================
| C++             | 508.namd_r(base, peak) 510.parest_r(base, peak) |
| icpc (ICC) 18.0.0 20170811 |
| Copyright (C) 1985-2017 Intel Corporation. All rights reserved. |

==============================================================================
| C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak) |

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

SPECrate®2017_fp_base = 69.7
SPECrate®2017_fp_peak = 71.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Compiler Version Notes (Continued)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
==============================================================================
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
         554.roms_r(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

SPECrater®2017_fp_base = 69.7
SPECrater®2017_fp_peak = 71.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Base Optimization Flags (Continued)

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Base Other Flags

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using both C and C++:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

SPECrate\textsuperscript{\copyright}2017 \_fp\_base = 69.7
SPECrate\textsuperscript{\copyright}2017 \_fp\_peak = 71.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Compiler Invocation (Continued)

Benmarks using both Fortran and C:
ifort icc

Benmarks using both C and C++:
icpc icc

Benmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm\_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

538.imagick\_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

544.nab\_r: Same as 519.lbm\_r

C++ benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:
503.bwaves\_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
-nostandard-realloc-lhs -align array32byte

549.fotonik3d\_r: Same as 503.bwaves\_r

554.roms\_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

SPECrate®2017_fp_base = 69.7
SPECrate®2017_fp_peak = 71.9

Peak Optimization Flags (Continued)

554.roms_r (continued):
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Peak Other Flags

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using both C and C++:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5122, 3.60 GHz)

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</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-12-08 18:33:28-0500.
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