### Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>203</td>
<td>207</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>503.bwaves_r</td>
<td>88</td>
</tr>
<tr>
<td>20</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>50</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>100</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>150</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>200</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>250</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>300</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>350</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>400</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>450</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
<tr>
<td>500</td>
<td>503.bwaves_r</td>
<td>195</td>
</tr>
</tbody>
</table>

---

### Hardware

- **CPU Name:** Intel Xeon Gold 6152  
- **Max MHz:** 3700  
- **Nominal:** 2100  
- **Enabled:** 44 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 30.25 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)  
- **Storage:** 1 x 600 GB SAS HDD, 10K RPM  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default  
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux  
- **Parallel:** No  
- **Firmware:** Version 3.1.1d released Jun-2017  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** None  
- **Power Management:** --
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 203
SPECrate®2017_fp_peak = 207

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>88</td>
<td>1789</td>
<td>493</td>
<td>1791</td>
<td>493</td>
<td>1790</td>
<td>493</td>
<td>88</td>
<td>1789</td>
<td>493</td>
<td>1793</td>
<td>492</td>
<td>1788</td>
<td>493</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>88</td>
<td>572</td>
<td>195</td>
<td>571</td>
<td>195</td>
<td>572</td>
<td>195</td>
<td>88</td>
<td>580</td>
<td>192</td>
<td>581</td>
<td>192</td>
<td>580</td>
<td>192</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>88</td>
<td>498</td>
<td>168</td>
<td>500</td>
<td>167</td>
<td>501</td>
<td>167</td>
<td>88</td>
<td>495</td>
<td>169</td>
<td>493</td>
<td>170</td>
<td>494</td>
<td>169</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>88</td>
<td>782</td>
<td>263</td>
<td>783</td>
<td>262</td>
<td>780</td>
<td>263</td>
<td>88</td>
<td>659</td>
<td>312</td>
<td>658</td>
<td>312</td>
<td>659</td>
<td>312</td>
</tr>
<tr>
<td>519.llvm_r</td>
<td>88</td>
<td>791</td>
<td>117</td>
<td>791</td>
<td>117</td>
<td>790</td>
<td>117</td>
<td>88</td>
<td>771</td>
<td>120</td>
<td>770</td>
<td>120</td>
<td>770</td>
<td>120</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>88</td>
<td>907</td>
<td>217</td>
<td>903</td>
<td>218</td>
<td>906</td>
<td>218</td>
<td>88</td>
<td>903</td>
<td>218</td>
<td>900</td>
<td>219</td>
<td>902</td>
<td>218</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>88</td>
<td>573</td>
<td>234</td>
<td>573</td>
<td>234</td>
<td>574</td>
<td>233</td>
<td>88</td>
<td>567</td>
<td>236</td>
<td>567</td>
<td>236</td>
<td>567</td>
<td>236</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>88</td>
<td>640</td>
<td>240</td>
<td>641</td>
<td>240</td>
<td>641</td>
<td>240</td>
<td>88</td>
<td>634</td>
<td>243</td>
<td>634</td>
<td>243</td>
<td>635</td>
<td>243</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>88</td>
<td>638</td>
<td>343</td>
<td>636</td>
<td>344</td>
<td>638</td>
<td>343</td>
<td>88</td>
<td>638</td>
<td>343</td>
<td>638</td>
<td>343</td>
<td>637</td>
<td>344</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>88</td>
<td>482</td>
<td>307</td>
<td>482</td>
<td>307</td>
<td>482</td>
<td>307</td>
<td>88</td>
<td>473</td>
<td>313</td>
<td>474</td>
<td>312</td>
<td>473</td>
<td>313</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>88</td>
<td>2320</td>
<td>148</td>
<td>2323</td>
<td>148</td>
<td>2320</td>
<td>148</td>
<td>88</td>
<td>2324</td>
<td>148</td>
<td>2320</td>
<td>148</td>
<td>2323</td>
<td>148</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>88</td>
<td>1510</td>
<td>92.6</td>
<td>1508</td>
<td>92.7</td>
<td>1514</td>
<td>92.4</td>
<td>88</td>
<td>1465</td>
<td>95.5</td>
<td>1474</td>
<td>94.9</td>
<td>1466</td>
<td>95.4</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

SPECrate®2017_fp_base = 203
SPECrate®2017_fp_peak = 207

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

General Notes (Continued)

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc09c0f
running on linux-ox2h Wed Dec 20 06:25:14 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6152 CPU @ 2.10GHz
  2 "physical id"s (chips)
  88 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 22
siblings : 44
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28

From lscpu:

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 88
On-line CPU(s) list: 0-87
Thread(s) per core: 2
Core(s) per socket: 22
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6152 CPU @ 2.10GHz
Stepping: 4
CPU MHz: 1405.760
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4190.14
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 30976K
NUMA node0 CPU(s): 0-2, 6-8, 11-13, 17, 18, 44-46, 50-52, 55-57, 61, 62
NUMA node1 CPU(s): 3-5, 9, 10, 14-16, 19-21, 47-49, 53, 54, 58-60, 63-65
NUMA node2 CPU(s): 22-24, 28-30, 33-35, 39, 40, 66-68, 72-74, 77-79, 83, 84
NUMA node3 CPU(s): 25-27, 31, 32, 36-38, 41-43, 69-71, 75, 76, 80-82, 85-87
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtopr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vnni fplibx86 ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrms invpcid rtm cmp cmx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occupp_l1c

/proc/cpuinfo cache data
  cache size : 30976 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 6 7 8 11 12 13 17 18 44 45 46 50 51 52 55 56 57 61 62
  node 0 size: 95258 MB
  node 0 free: 94822 MB

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

SPECrate®2017_fp_base = 203
SPECrate®2017_fp_peak = 207

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

node 1 cpus: 3 4 5 9 10 14 15 16 19 20 21 47 48 49 53 54 58 59 60 63 64 65
node 1 size: 96760 MB
node 1 free: 96327 MB
node 2 cpus: 22 23 24 28 29 30 33 34 35 39 40 66 67 68 72 73 74 77 78 79 83 84
node 2 size: 96760 MB
node 2 free: 96433 MB
node 3 cpus: 25 26 27 31 32 36 37 38 41 42 43 69 70 71 75 76 80 81 82 85 86 87
node 3 size: 96624 MB
node 3 free: 96276 MB
node distances:
  node 0 1 2 3
  0: 10 11 21 21
  1: 11 10 21 21
  2: 21 21 10 11
  3: 21 21 11 10

From /proc/meminfo
MemTotal: 394653104 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-ox2h 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 18 20:36

SPEC is set to: /home/cpu2017
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

SPECrater®2017_fp_base = 203
SPECrater®2017_fp_peak = 207

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sdb5      xfs   317G   98G  220G  31% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

---------------------------------------------------------------------------------------------------------------
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
               | 544.nab_r(base, peak)
---------------------------------------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
---------------------------------------------------------------------------------------------------------------
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
---------------------------------------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
---------------------------------------------------------------------------------------------------------------
C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak)
---------------------------------------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
---------------------------------------------------------------------------------------------------------------
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
---------------------------------------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

| SPECrate®2017_fp_base = 203 |
| SPECrate®2017_fp_peak = 207 |

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

---

**Compiler Version Notes (Continued)**

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
| 554.roms_r(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

**Base Compiler Invocation**

C benchmarks:
  icc

C++ benchmarks:
  icpc

Fortran benchmarks:
  ifort

Benchmarks using both Fortran and C:
  ifort icc

Benchmarks using both C and C++:
  icpc icc

Benchmarks using Fortran, C, and C++:
  icpc icc ifort
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

| SPECrate®2017_fp_base | 203 |
| SPECrate®2017_fp_peak | 207 |

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Test Date:** Dec-2017
**Tested by:** Cisco Systems
**Hardware Availability:** Aug-2017
**Software Availability:** Sep-2017

### Base Portability Flags

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3

**C++ benchmarks:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3

**Fortran benchmarks:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

**Benchmarks using both Fortran and C:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

**Benchmarks using both C and C++:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3

**Benchmarks using Fortran, C, and C++:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

SPECrate®2017_fp_base = 203
SPECrate®2017_fp_peak = 207

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Dec-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Sep-2017</td>
</tr>
</tbody>
</table>

Base Other Flags

C benchmarks:
- m64 -std=c11

C++ benchmarks:
- m64

Fortran benchmarks:
- m64

Benchmarks using both Fortran and C:
- m64 -std=c11

Benchmarks using both C and C++:
- m64 -std=c11

Benchmarks using Fortran, C, and C++:
- m64 -std=c11

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

**SPECrate®2017_fp_base = 203**

**SPECrate®2017_fp_peak = 207**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2017</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

### Peak Optimization Flags

#### C benchmarks:

- 519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
  -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=3

- 538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=3

- 544.nab_r: Same as 519.lbm_r

#### C++ benchmarks:

- -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
  -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=3

#### Fortran benchmarks:

- 503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=3

- 549.fotonik3d_r: Same as 503.bwaves_r

- 554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
  -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

#### Benchmarks using both Fortran and C:

- -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
  -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

#### Benchmarks using both C and C++:

- -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
  -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=3

#### Benchmarks using Fortran, C, and C++:

- -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
  -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6152, 2.10 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Cisco Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>SPECrate&lt;sup&gt;®&lt;/sup&gt;2017_fp_base = 203</td>
<td></td>
</tr>
<tr>
<td>SPECrate&lt;sup&gt;®&lt;/sup&gt;2017_fp_peak = 207</td>
<td></td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2017</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

### Peak Other Flags

C benchmarks:
- `-m64 -std=c11`

C++ benchmarks:
- `-m64`

Fortran benchmarks:
- `-m64`

Benchmarks using both Fortran and C:
- `-m64 -std=c11`

Benchmarks using both C and C++:
- `-m64 -std=c11`

Benchmarks using Fortran, C, and C++:
- `-m64 -std=c11`

The flags files that were used to format this result can be browsed at
- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:
- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU<sup>®</sup>2017 v1.0.2 on 2017-12-20 09:25:13-0500.
Report generated on 2020-08-05 14:21:02 by CPU2017 PDF formatter v6255.
Originally published on 2018-02-23.