Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater2017_int_base = 34.1
SPECrater2017_int_peak = 34.9

<table>
<thead>
<tr>
<th>Test Date: Dec-2017</th>
<th>Hardware Availability: Aug-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software Availability: Jun-2017</td>
<td></td>
</tr>
</tbody>
</table>

**CPU Name:** Intel Xeon Bronze 3104  
**Max MHz.:** 1700

**Nominal:** 1700  
**Enabled:** 12 cores, 2 chips  
**Orderable:** 1,2 Chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 8.25 MB I+D on chip per chip  
**Other:** None  
**Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2133)  
**Storage:** 1 x 600 GB SAS HDD, 10K RPM  
**Other:** None

**OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)  
**Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux  
**Parallel:** No  
**Firmware:** Version 3.1.1d released Jun-2017  
**System State:** Run level 3 (multi-user)  
**File System:** xfs  
**Base Pointers:** 64-bit  
**Peak Pointers:** 32/64-bit  
**Other:** jemalloc: jemalloc memory allocator library V5.0.1; jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets; jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5; jemalloc: sources available from jemalloc.net or releases
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

SPECrate2017_int_base = 34.1
SPECrate2017_int_peak = 34.9

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perbench_r</td>
<td>12</td>
<td>674</td>
<td>28.3</td>
<td>677</td>
<td>28.2</td>
<td>678</td>
<td>28.2</td>
<td>12</td>
<td>576</td>
<td>33.2</td>
<td>577</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>12</td>
<td>513</td>
<td>33.1</td>
<td>514</td>
<td>33.1</td>
<td>514</td>
<td>33.1</td>
<td>12</td>
<td>450</td>
<td>37.8</td>
<td>451</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>12</td>
<td>500</td>
<td>38.8</td>
<td>500</td>
<td>38.8</td>
<td>500</td>
<td>38.8</td>
<td>12</td>
<td>500</td>
<td>38.8</td>
<td>500</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>12</td>
<td>642</td>
<td>24.5</td>
<td>639</td>
<td>24.6</td>
<td>639</td>
<td>24.7</td>
<td>12</td>
<td>634</td>
<td>24.8</td>
<td>631</td>
</tr>
<tr>
<td>523.xalanckm_r</td>
<td>12</td>
<td>351</td>
<td>36.1</td>
<td>352</td>
<td>36.0</td>
<td>351</td>
<td>36.1</td>
<td>12</td>
<td>323</td>
<td>39.2</td>
<td>324</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>12</td>
<td>305</td>
<td>68.9</td>
<td>305</td>
<td>69.0</td>
<td>305</td>
<td>68.9</td>
<td>12</td>
<td>357</td>
<td>58.8</td>
<td>358</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>12</td>
<td>486</td>
<td>28.3</td>
<td>486</td>
<td>28.3</td>
<td>486</td>
<td>28.3</td>
<td>12</td>
<td>486</td>
<td>28.3</td>
<td>485</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>12</td>
<td>859</td>
<td>23.1</td>
<td>859</td>
<td>23.1</td>
<td>859</td>
<td>23.1</td>
<td>12</td>
<td>854</td>
<td>23.3</td>
<td>854</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>12</td>
<td>483</td>
<td>65.1</td>
<td>483</td>
<td>65.1</td>
<td>483</td>
<td>65.1</td>
<td>12</td>
<td>484</td>
<td>64.9</td>
<td>483</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>12</td>
<td>580</td>
<td>22.4</td>
<td>579</td>
<td>22.4</td>
<td>579</td>
<td>22.4</td>
<td>12</td>
<td>579</td>
<td>22.4</td>
<td>579</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

SPECrate2017_int_base = 34.1
SPECrate2017_int_peak = 34.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Platform Notes

BIOS Settings:
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b091c0f
running on linux-ox2h Fri Dec 15 18:45:39 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
  2 "physical id"s (chips)
  12 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 6
    siblings : 6
    physical 0: cores 0 1 2 3 4 5
    physical 1: cores 0 1 2 3 4 5

From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 12

(Continued on next page)
Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>34.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_int_peak</td>
<td>34.9</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Dec-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability: Aug-2017</td>
<td></td>
</tr>
<tr>
<td>Software Availability: Jun-2017</td>
<td></td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

- On-line CPU(s) list: 0-11
- Thread(s) per core: 1
- Core(s) per socket: 6
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
- Stepping: 4
- CPU MHz: 1263.776
- CPU max MHz: 1700.0000
- CPU min MHz: 800.0000
- BogoMIPS: 3392.02
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 8448K
- NUMA node0 CPU(s): 0-5
- NUMA node1 CPU(s): 6-11
- Flags: fpu vme de pse ts mce pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mpx mmx sbx ssh ht tm pbe syscall nx pdpe1gb rdtscp lm constant tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop tsc aperfmpref perf eagerpfn phi pmlmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch arat epb pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3rms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

Available:nodes (0-1)
node 0 cpus: 0 1 2 3 4 5
node 0 size: 192019 MB
node 0 free: 187567 MB
node 1 cpus: 6 7 8 9 10 11
node 1 size: 193384 MB
node 1 free: 190912 MB
node distances:
node 0 1
0: 10 21

(Continued on next page)
Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>34.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_int_peak</td>
<td>34.9</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

```
1:  21  10

From /proc/meminfo
  MemTotal:       394653944 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

/usr/bin/lsb_release -d
  SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-ox2h 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 14 03:35

SPEC is set to: /home/cpu2017
  Filesystem   Type  Size  Used Avail Use% Mounted on
  /dev/sdb5    xfs  317G  99G  218G  32% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
  Memory:
    24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2133

(End of data from sysinfo program)
```
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

SPECrate2017_int_base = 34.1
SPECrate2017_int_peak = 34.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jun-2017

Compiler Version Notes
==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
    525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
  icc (ICC) 18.0.0 20170811
  Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
CC  500.perlbench_r(peak) 502.gcc_r(peak)
==============================================================================
  icc (ICC) 18.0.0 20170811
  Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
    541.leela_r(base)
==============================================================================
  icpc (ICC) 18.0.0 20170811
  Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
    541.leela_r(peak)
==============================================================================
  icpc (ICC) 18.0.0 20170811
  Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
FC  548.exchange2_r(base, peak)
==============================================================================
  ifort (IFORT) 18.0.0 20170811
  Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation
C benchmarks:
  icc

C++ benchmarks:
  icpc

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

| SPECrate2017_int_base | 34.1 |
| SPECrate2017_int_peak | 34.9 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbmk_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Base Other Flags

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

(Continued on next page)
Base Other Flags (Continued)

Fortran benchmarks:

- m64

Peak Compiler Invocation

C benchmarks:

icc

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
   -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
   -fno-strict-overflow -L/usr/local/je5.0.1-64/lib
   -ljemalloc

502.gcc_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
   -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
   -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
   -L/usr/local/je5.0.1-32/lib -ljemalloc
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

| SPECrate2017_int_base | 34.1 |
| SPECrate2017_int_peak | 34.9 |

Peak Optimization Flags (Continued)

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib
-ljemalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/usr/local/je5.0.1-64/lib -ljemalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-64/lib -ljemalloc

523.xalancbmk_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Other Flags

C benchmarks (except as noted below):
-m64 -std=c11

502.gcc_r: -m32 -std=c11

C++ benchmarks (except as noted below):
-m64

523.xalancbmk_r: -m32

(Continued on next page)
SPEC CPU2017 Integer Rate Result

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

| SPECrate2017_int_base = 34.1 |
| SPECrate2017_int_peak = 34.9 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jun-2017

Fortran benchmarks:
- m64

Peak Other Flags (Continued)

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2017-12-15 21:45:38-0500.
Originally published on 2018-02-23.