## Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>149</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_int_peak</td>
<td>157</td>
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</tbody>
</table>

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<tr>
<th>CPU2017 License:</th>
<th>9019</th>
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<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
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<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2017</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Jul-2017</td>
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</tbody>
</table>

### Hardware

<table>
<thead>
<tr>
<th>CPU Name</th>
<th>Intel Xeon Gold 6136</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max MHz:</td>
<td>3700</td>
</tr>
<tr>
<td>Nominal:</td>
<td>3000</td>
</tr>
<tr>
<td>Enabled:</td>
<td>24 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>24.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Memory:</td>
<td>384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 600 GB SAS HDD, 10K RPM</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 3.2.1d released Jul-2017</td>
</tr>
<tr>
<td>File System:</td>
<td>xfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other:</td>
<td>jemalloc: jemalloc memory allocator library V5.0.1; jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets; jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5; jemalloc: sources avilable from jemalloc.net or releases</td>
</tr>
</tbody>
</table>

---

### Results

<table>
<thead>
<tr>
<th>Test</th>
<th>SPECrate2017_int_base</th>
<th>SPECrate2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>137</td>
<td>157</td>
</tr>
<tr>
<td>gcc_r</td>
<td>129</td>
<td>157</td>
</tr>
<tr>
<td>mcf_r</td>
<td>183</td>
<td>184</td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>156</td>
<td>184</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>129</td>
<td>312</td>
</tr>
<tr>
<td>x264_r</td>
<td>129</td>
<td>129</td>
</tr>
<tr>
<td>deepsjeng_r</td>
<td>127</td>
<td>127</td>
</tr>
<tr>
<td>leela_r</td>
<td>126</td>
<td>126</td>
</tr>
<tr>
<td>exchange2_r</td>
<td>156</td>
<td>126</td>
</tr>
<tr>
<td>xz_r</td>
<td>126</td>
<td>289</td>
</tr>
</tbody>
</table>

---

**Graph: CPU2017 Integer Rate Result**

- **SPECrate2017_int_base**:
  - 149
- **SPECrate2017_int_peak**:
  - 157

---

Page 1: Standard Performance Evaluation Corporation (info@spec.org) 
https://www.spec.org/
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECrate2017_int_base = 149
SPECrate2017_int_peak = 157

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>48</td>
<td>692</td>
<td>110</td>
<td>688</td>
<td>111</td>
<td>684</td>
<td>112</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>48</td>
<td>525</td>
<td>129</td>
<td>525</td>
<td>129</td>
<td>533</td>
<td>128</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>48</td>
<td>410</td>
<td>189</td>
<td>423</td>
<td>183</td>
<td>428</td>
<td>181</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>48</td>
<td>711</td>
<td>88.6</td>
<td>720</td>
<td>87.5</td>
<td>713</td>
<td>88.4</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>48</td>
<td>323</td>
<td>157</td>
<td>325</td>
<td>156</td>
<td>326</td>
<td>156</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>48</td>
<td>269</td>
<td>313</td>
<td>269</td>
<td>312</td>
<td>270</td>
<td>311</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>48</td>
<td>423</td>
<td>130</td>
<td>425</td>
<td>129</td>
<td>426</td>
<td>129</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>48</td>
<td>647</td>
<td>123</td>
<td>631</td>
<td>126</td>
<td>632</td>
<td>126</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>48</td>
<td>435</td>
<td>289</td>
<td>435</td>
<td>289</td>
<td>436</td>
<td>289</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>48</td>
<td>484</td>
<td>107</td>
<td>520</td>
<td>99.7</td>
<td>522</td>
<td>99.3</td>
</tr>
</tbody>
</table>

Submit Notes
The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on

(Continued on next page)
General Notes (Continued)

past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-mys2 Mon Dec 18 00:42:29 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6136 CPU @ 3.00GHz
 2 "physical id"s (chips)
 48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 24
physical 0: cores 0 1 2 3 4 8 9 11 17 18 19 20
physical 1: cores 0 1 4 9 10 11 17 18 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian

(Continued on next page)
Platform Notes (Continued)

CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6136 CPU @ 3.00GHz
Stepping: 4
CPU MHz: 2705.086
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 5999.98
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-11,24-35
NUMA node1 CPU(s): 12-23,36-47
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt pckeopt specmem mce lms hook mmx2 fxsr32 aes xsave f16c rdrand load.lat lhfl_lm abm 3nowprefetch ida arat epb pln pts dtherm hwp hwp_act_window hwp_epp hwp_kpr_req intel_pit tpr_shadow vmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512v1 xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

   available: 2 nodes (0-1)
   node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 24 25 26 27 28 29 30 31 32 33 34 35
   node 0 size: 192074 MB
   node 0 free: 185077 MB
   node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 36 37 38 39 40 41 42 43 44 45 46 47
   node 1 size: 193504 MB
   node 1 free: 187615 MB
   node distances:
      node 0 1

(Continued on next page)
Cisco Systems
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SPECrate2017_int_peak = 157

Platform Notes (Continued)

0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 394832372 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.

os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-mys2 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 11 16:15

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used Avail Use% Mounted on
  /dev/sda3    xfs  182G  33G  150G  18%  /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
  Memory:
    24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)
Cisco Systems  
Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)  

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</tbody>
</table>

**SPEC CPU2017 Integer Rate Result**

**SPECrate2017_int_base = 149**

**SPECrate2017_int_peak = 157**

---

### Compiler Version Notes

```
==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
    525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
```

```
==============================================================================
CC  500.perlbench_r(peak) 502.gcc_r(peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
```

```
==============================================================================
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
    541.leela_r(base)
==============================================================================
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
```

```
==============================================================================
CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
    541.leela_r(peak)
==============================================================================
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
```

```
==============================================================================
FC  548.exchange2_r(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
```

---

### Base Compiler Invocation

C benchmarks:

- icc

C++ benchmarks:

- icpc

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Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)

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Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r -DSPEC_LP64
505.mcf_r -DSPEC_LP64
520.omnetpp_r -DSPEC_LP64
523.xalancbmk_r -DSPEC_LP64 -DSPEC_LINUX
525.x264_r -DSPEC_LP64
531.deepsjeng_r -DSPEC_LP64
541.leela_r -DSPEC_LP64
548.exchange2_r -DSPEC_LP64
557.xz_r -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Base Other Flags

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

(Continued on next page)
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Base Other Flags (Continued)

Fortran benchmarks:
-m64

Peak Compiler Invocation

C benchmarks:
icc
C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

(Continued on next page)

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib
-ljemalloc

502.gcc_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

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Peak Optimization Flags (Continued)

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib
-ljemalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/usr/local/je5.0.1-64/lib -ljemalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-64/lib -ljemalloc

523.xalancbmk_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Other Flags

C benchmarks (except as noted below):
-m64 -std=c11

502.gcc_r: -m32 -std=c11

C++ benchmarks (except as noted below):
-m64

523.xalancbmk_r: -m32

(Continued on next page)
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</table>

### Peak Other Flags (Continued)

Fortran benchmarks:

```
-m64
```

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

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