## Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3106, 1.70 GHz)

<table>
<thead>
<tr>
<th>SPECrate2017_int_base = 45.5</th>
<th>SPECrate2017_int_peak = 46.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License: 9019</td>
<td>Test Date: Dec-2017</td>
</tr>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Jul-2017</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)</td>
<td>CPU Name: Intel Xeon Bronze 3106</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 18.0.0.128 of Intel C/C++</td>
<td>Max MHz.: 1700</td>
</tr>
<tr>
<td>Compiler for Linux: Fortran: Version 18.0.0.128 of Intel Fortran</td>
<td>Nominal: 1700</td>
</tr>
<tr>
<td>Firmware: Version 3.2.1d released Jul-2017</td>
<td>Enabled: 16 cores, 2 chips</td>
</tr>
<tr>
<td>File System: xfs</td>
<td>Orderable: 1,2 Chips</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
<td>L3: 11 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other: jemalloc: jemalloc memory allocator library V5.0.1; jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets; jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5; jemalloc: sources avilable from jemalloc.net or releases</td>
<td>Other: None</td>
</tr>
</tbody>
</table>

### Copies

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<thead>
<tr>
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<th>Software Availability: Jul-2017</th>
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<tr>
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<td>SPECrate2017_int_base (45.5)</td>
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<td>502.gcc_r</td>
<td>SPECrate2017_int_peak (46.6)</td>
</tr>
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<td>505.mcf_r</td>
<td></td>
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</tr>
<tr>
<td>525.x264_r</td>
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<tr>
<td>531.deepsjeng_r</td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td></td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td></td>
</tr>
<tr>
<td>557.zx_r</td>
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</table>

### CPU Name: Intel Xeon Bronze 3106
Max MHz.: 1700
Nominal: 1700
Enabled: 16 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 11 MB I+D on chip per chip
Other: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2133)
Storage: 1 x 600 GB SAS HDD, 10K RPM
Other: None

### Test Date: Dec-2017
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### Cisco Systems

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### Results Table

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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>500.perlbench_r</td>
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<td>44.6</td>
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<td>44.6</td>
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<tr>
<td>505.mcf_r</td>
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<tr>
<td>520.omnetpp_r</td>
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<td>92.2</td>
<td>304</td>
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<td>856</td>
<td>30.9</td>
<td>857</td>
<td>30.9</td>
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<td>87.0</td>
<td>483</td>
<td>86.8</td>
<td>482</td>
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<tr>
<td>557.xz_r</td>
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<td>29.8</td>
<td>580</td>
<td>29.8</td>
<td>580</td>
<td>29.8</td>
</tr>
</tbody>
</table>

---

### Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### General Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
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---

**General Notes (Continued)**

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

---

**Platform Notes**

**BIOS Settings:**
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Disabled  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b091c0f  
running on linux Sat Dec 16 08:46:38 2017

**SUT (System Under Test) info as seen by some common utilities.**
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Bronze 3106 CPU @ 1.70GHz  
2 "physical id"s (chips)  
16 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 8  
siblings : 8  
physical 0: cores 0 1 2 3 4 5 6 7  
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:  
Architecture: x86_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 16

---

(Continued on next page)
SPEC CPU2017 Integer Rate Result

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Platform Notes (Continued)

On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Bronze 3106 CPU @ 1.70GHz
Stepping: 4
CPU MHz: 1582.672
CPU max MHz: 1700.0000
CPU min MHz: 800.0000
BogoMIPS: 3399.98
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmprefl eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpmr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow flexpriority ept vpid
fsgbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnowprec fetch arat epb pln pts dtherm hwp
/node_cpuinfo cache data
   cache size: 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7
  node 0 size: 191913 MB
  node 0 free: 188412 MB
  node 1 cpus: 8 9 10 11 12 13 14 15
  node 1 size: 193504 MB
  node 1 free: 189552 MB
  node distances:
  node 0 1
  0: 10 21

(Continued on next page)
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Platform Notes (Continued)

1:  21  10

From /proc/meminfo

| MemTotal:       | 394667604 kB |
| MemTotal:       | 394667604 kB |
| HugePages_Total:| 0            |
| Hugepagesize:   | 2048 kB      |

From /etc/*release*  

<table>
<thead>
<tr>
<th>SuSE-release:</th>
</tr>
</thead>
<tbody>
<tr>
<td>SuSE Linux Enterprise Server 12 (x86_64)</td>
</tr>
<tr>
<td>VERSION = 12</td>
</tr>
<tr>
<td>PATCHLEVEL = 2</td>
</tr>
<tr>
<td># This file is deprecated and will be removed in a future service pack or release.</td>
</tr>
<tr>
<td># Please check /etc/os-release for details about this release.</td>
</tr>
<tr>
<td>os-release:</td>
</tr>
<tr>
<td>NAME=&quot;SLES&quot;</td>
</tr>
<tr>
<td>VERSION=&quot;12-SP2&quot;</td>
</tr>
<tr>
<td>VERSION_ID=&quot;12.2&quot;</td>
</tr>
<tr>
<td>PRETTY_NAME=&quot;SUSE Linux Enterprise Server 12 SP2&quot;</td>
</tr>
<tr>
<td>ID=&quot;sles&quot;</td>
</tr>
<tr>
<td>ANSI_COLOR=&quot;0;32&quot;</td>
</tr>
<tr>
<td>CPE_NAME=&quot;cpe:/o:suse:sles:12:sp2&quot;</td>
</tr>
</tbody>
</table>

uname -a:

| Linux linux 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67) x86_64 |
| x86_64 x86_64 GNU/Linux |

run-level 3 Jan 2 13:39

SPEC is set to: /home/cpu2017  
FileSystem Type Size Used Avail Use% Mounted on  
/dev/sda1 xfs 280G 144G 136G 52% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard. 

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:

24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2133

(End of data from syssinfo program)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3106, 1.70 GHz)

SPEC CPU2017 Integer Rate Result
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Cisco UCS B200 M5 (Intel Xeon Bronze 3106, 1.70 GHz)

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SPECrate2017_int_peak = 46.6

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jul-2017

Compiler Version Notes
==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
  525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

CC  500.perlbench_r(peak) 502.gcc_r(peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
  541.leela_r(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
  541.leela_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

FC  548.exchange2_r(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation
C benchmarks:
  icc
C++ benchmarks:
  icpc

(Continued on next page)
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Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Base Other Flags

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

(Continued on next page)
## SPEC CPU2017 Integer Rate Result

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### Base Other Flags (Continued)

- Fortran benchmarks:  
  - m64

### Peak Compiler Invocation

- C benchmarks:  
  - icc
- C++ benchmarks:  
  - icpc
- Fortran benchmarks:  
  - ifort

### Peak Portability Flags

- 500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
- 502.gcc_r: -D_FILE_OFFSET_BITS=64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64

### Peak Optimization Flags

- C benchmarks:  
  - 500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -fno-strict-overflow -L/usr/local/je5.0.1-64/lib -ljemalloc

(Continued on next page)
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Peak Optimization Flags (Continued)

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib
-ljemalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/usr/local/je5.0.1-64/lib -ljemalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-64/lib -ljemalloc

523.xalancbmk_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Other Flags

C benchmarks (except as noted below):
-m64 -std=c11

502.gcc_r: -m32 -std=c11

C++ benchmarks (except as noted below):
-m64

523.xalancbmk_r: -m32

(Continued on next page)
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Peak Other Flags (Continued)

Fortran benchmarks:
- m64

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml