Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
CPU Name: Intel Xeon Silver 4108
Max MHz: 3000
Nominal: 1800
Enabled: 16 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 11 MB I+D on chip per core
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)
Storage: 1 x 600 GB SAS HDD, 10K RPM
Other: None

Software
OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 3.2.1d released Jul-2017
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: --

SPECspeed®2017_fp_base = 56.5
SPECspeed®2017_fp_peak = 57.0

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base (56.5)</th>
<th>SPECspeed®2017_fp_peak (57.0)</th>
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<tbody>
<tr>
<td>16</td>
<td>69.5</td>
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<td>16</td>
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<td>16</td>
<td>61.7</td>
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</table>

---

603.bwaves_s
607.cactuBSSN_s
619.lbm_s
621.wrf_s
627.cam4_s
628.pop2_s
638.imagick_s
644.nab_s
649.fotonik3d_s
654.roms_s
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>621.wrf_s</td>
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<td>644.nab_s</td>
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<td>65.2</td>
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<td>65.2</td>
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<td>649.fotonik3d_s</td>
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<td>222</td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 56.5
SPECspeed®2017_fp_peak = 57.0

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.
The system as described on this result page was formerly

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPEC CPU®2017 Floating Point Speed Result

SPECspeed®2017_fp_base = 56.5
SPECspeed®2017_fp_peak = 57.0

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<td>Hardware Availability: Aug-2017</td>
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<tr>
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<td>Software Availability: Sep-2017</td>
</tr>
</tbody>
</table>

General Notes (Continued)

generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-djj4 Sun Dec 17 16:35:18 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 8
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

**SPEC CPU®2017 Floating Point Speed Result**

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<table>
<thead>
<tr>
<th>Platform Notes (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NUMA node(s):</td>
</tr>
<tr>
<td>Vendor ID:</td>
</tr>
<tr>
<td>CPU family:</td>
</tr>
<tr>
<td>Model:</td>
</tr>
<tr>
<td>Model name:</td>
</tr>
<tr>
<td>Stepping:</td>
</tr>
<tr>
<td>CPU MHZ:</td>
</tr>
<tr>
<td>CPU max MHZ:</td>
</tr>
<tr>
<td>CPU min MHZ:</td>
</tr>
<tr>
<td>BogoMIPS:</td>
</tr>
<tr>
<td>Virtualization:</td>
</tr>
<tr>
<td>L1d cache:</td>
</tr>
<tr>
<td>L1i cache:</td>
</tr>
<tr>
<td>L2 cache:</td>
</tr>
<tr>
<td>L3 cache:</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
</tr>
<tr>
<td>Flags:</td>
</tr>
</tbody>
</table>

/proc/cpuinfo cache data

cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)

node 0 cpus: 0 1 2 3 4 5 6 7
node 0 size: 191913 MB
node 0 free: 188282 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 193504 MB
node 1 free: 188991 MB
node distances:

distance:

node 0:

0: 10 21
1: 21 10

From /proc/meminfo

MemTotal: 394667604 kB

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

**Platform Notes (Continued)**

HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-djj4 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 4 06:54

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda1</td>
<td>xfs</td>
<td>559G</td>
<td>129G</td>
<td>430G</td>
<td>24%</td>
<td>/</td>
</tr>
</tbody>
</table>

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
    24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

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**Compiler Version Notes**

```
--------------------------
 C                    | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
                      | 644.nab_s(base, peak)
--------------------------
```

icc (ICC) 18.0.0 20170811

(Continued on next page)
Cisco Systems  
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)  

**SPECs**
- SPECs**2017_fp_base = 56.5**  
- SPECs**2017_fp_peak = 57.0**  

**CPU2017 License:** 9019  
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**Hardware Availability:** Aug-2017  
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**Software Availability:** Sep-2017

**Compiler Version Notes (Continued)**

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C++, C, Fortran | 607.cactuBSSN_s(base, peak)

---

icpc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

icc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

ifort (IFORT) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

Fortran | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak) 654.roms_s(base, peak)

---

ifort (IFORT) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

Fortran, C | 621.wrf_s(base, peak) 627.cam4_s(base, peak) 628.pop2_s(base, peak)

---

ifort (IFORT) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

icc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

**Base Compiler Invocation**

C benchmarks:  
- icc

Fortran benchmarks:  
- ifort

Benchmarks using both Fortran and C:  
- ifort icc

Benchmarks using Fortran, C, and C++:  
- icpc icc ifort
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPECspeed®2017_fp_base = 56.5
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Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Base Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPECspeed\textsuperscript{®}2017\_fp\_base = 56.5
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Software Availability: Sep-2017

**Base Other Flags (Continued)**

Benchmarks using both Fortran and C:
\[-m64 -std=c11\]

Benchmarks using Fortran, C, and C++:
\[-m64 -std=c11\]

**Peak Compiler Invocation**

C benchmarks:
\texttt{icc}

Fortran benchmarks:
\texttt{ifort}

Benchmarks using both Fortran and C:
\texttt{ifort icc}

Benchmarks using Fortran, C, and C++:
\texttt{icpc icc ifort}

**Peak Portability Flags**

Same as Base Portability Flags

**Peak Optimization Flags**

C benchmarks:
619.lbm.s: -prof-gen(pass 1) -prof-use(pass 2) -o2 -xCORE-AVX512 -qopt-prefetch -ipo -o3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP

638.imagick.s: -xCORE-AVX512 -ipo -o3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

644.nab.s: Same as 638.imagick.s

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPEC CPU®2017 Floating Point Speed Result

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Peak Optimization Flags (Continued)

Fortran benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -02 -xCORE-AVX512 -gopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -gopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -02 -xCORE-AVX512
-gopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-gopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -02 -xCORE-AVX512 -gopt-prefetch
-ipo -O3 -ffinite-math-only -no-prec-div -gopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte

Peak Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html
## Cisco Systems

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You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-12-17 16:35:17-0500.  
Originally published on 2018-02-23.