Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECrate2017_int_base = 66.6</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SPECrate2017_int_peak = 69.2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hardware</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Silver 4108</td>
</tr>
<tr>
<td>Max MHz.:</td>
<td>3000</td>
</tr>
<tr>
<td>Nominal:</td>
<td>1800</td>
</tr>
<tr>
<td>Enabled:</td>
<td>16 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>11 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Memory:</td>
<td>384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 600 GB SAS HDD, 10K RPM</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
</tbody>
</table>

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |
| Test Date: | Dec-2017 |
| Hardware Availability: | Aug-2017 |
| Software Availability: | Jun-2017 |

### SPEC Integer Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate2017_int_base</th>
<th>SPECrate2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>32</td>
<td>48.9</td>
<td>69.2</td>
</tr>
<tr>
<td>gcc_r</td>
<td>32</td>
<td>45.6</td>
<td>62.0</td>
</tr>
<tr>
<td>mcf_r</td>
<td>32</td>
<td>50.1</td>
<td>71.3</td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>32</td>
<td>47.1</td>
<td>71.3</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>32</td>
<td>45.6</td>
<td>83.0</td>
</tr>
<tr>
<td>x264_r</td>
<td>32</td>
<td>50.5</td>
<td>81.4</td>
</tr>
<tr>
<td>deepsjeng_r</td>
<td>32</td>
<td>55.0</td>
<td>84.5</td>
</tr>
<tr>
<td>leela_r</td>
<td>32</td>
<td>50.6</td>
<td>122</td>
</tr>
<tr>
<td>exchange2_r</td>
<td>32</td>
<td>50.1</td>
<td>123</td>
</tr>
<tr>
<td>xz_r</td>
<td>32</td>
<td>50.6</td>
<td>119</td>
</tr>
</tbody>
</table>

---

**Hardware**

- **CPU Name:** Intel Xeon Silver 4108
- **Max MHz.:** 3000
- **Nominal:** 1800
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Storage:** 1 x 600 GB SAS HDD, 10K RPM
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 3.1.1d released Jun-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc: jemalloc memory allocator library V5.0.1;
  jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets;
  jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;
  jemalloc: sources available from jemalloc.net or releases
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPECrate2017_int_base = 66.6
SPECrate2017_int_peak = 69.2

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>1046</td>
<td>48.7</td>
<td>1039</td>
<td>49.0</td>
<td>1042</td>
<td>48.9</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>32</td>
<td>731</td>
<td>62.0</td>
<td>729</td>
<td>62.2</td>
<td>735</td>
<td>61.6</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>32</td>
<td>627</td>
<td>82.4</td>
<td>623</td>
<td>83.0</td>
<td>623</td>
<td>83.0</td>
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<tr>
<td>520.omnetpp_r</td>
<td>32</td>
<td>890</td>
<td>47.2</td>
<td>892</td>
<td>47.1</td>
<td>894</td>
<td>47.0</td>
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<td>523.xalancbmk_r</td>
<td>32</td>
<td>466</td>
<td>72.6</td>
<td>467</td>
<td>72.3</td>
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<td>72.0</td>
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<tr>
<td>525.x264_r</td>
<td>32</td>
<td>455</td>
<td>123</td>
<td>460</td>
<td>122</td>
<td>458</td>
<td>122</td>
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<tr>
<td>531.deepsjeng_r</td>
<td>32</td>
<td>667</td>
<td>55.0</td>
<td>667</td>
<td>55.0</td>
<td>667</td>
<td>55.0</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>32</td>
<td>1047</td>
<td>50.6</td>
<td>1051</td>
<td>50.4</td>
<td>1049</td>
<td>50.5</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>32</td>
<td>707</td>
<td>119</td>
<td>706</td>
<td>119</td>
<td>705</td>
<td>119</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>32</td>
<td>690</td>
<td>50.1</td>
<td>691</td>
<td>50.0</td>
<td>690</td>
<td>50.1</td>
</tr>
</tbody>
</table>

SPECrate2017_int_base = 66.6
SPECrate2017_int_peak = 69.2

Submit Notes
The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on (Continued on next page)
# SPEC CPU2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)  

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>66.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_int_peak</td>
<td>69.2</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

## General Notes (Continued)

past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

## Platform Notes

BIOS Settings:  
Intel HyperThreading Technology set to Enabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bce091c0f  
running on linux-3joc Sat Dec 16 06:44:39 2017

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo  
model name: Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz  
  2 "physical id"s (chips)  
  32 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores: 8  
siblings: 16  
physical 0: cores 0 1 2 3 4 5 6 7  
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:  
Architecture: x86_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian

(Continued on next page)
## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License</td>
<td>9019</td>
</tr>
<tr>
<td>Test Sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date</td>
<td>Dec-2017</td>
</tr>
<tr>
<td>Hardware Availability</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability</td>
<td>Jun-2017</td>
</tr>
</tbody>
</table>

 SPECrate2017_int_base = 66.6  
 SPECrate2017_int_peak = 69.2

### Platform Notes (Continued)

- **CPU(s):** 32
- **On-line CPU(s) list:** 0-31
- **Thread(s) per core:** 2
- **Core(s) per socket:** 8
- **Socket(s):** 2
- **NUMA node(s):** 2
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
- **Stepping:** 4
- **CPU MHz:** 2247.796
- **CPU max MHz:** 3000.0000
- **CPU min MHz:** 800.0000
- **BogoMIPS:** 3591.56
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 11264K
- **NUMA node0 CPU(s):** 0-7,16-23
- **NUMA node1 CPU(s):** 8-15,24-31
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu nni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrp pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2  3dnowprocratio cpuid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_11c cqm_occup_llc

From numactl --hardware

```
 WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

<table>
<thead>
<tr>
<th>Available Nodes</th>
<th>CPU(s)</th>
<th>Size</th>
<th>Free</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>32</td>
<td>11264 KB</td>
<td></td>
</tr>
</tbody>
</table>

```bash
proc/cpuinfo cache data
cache size : 11264 KB
```

From numactl --hardware
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPECrate2017_int_base = 66.6
SPECrate2017_int_peak = 69.2

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2017
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Jun-2017

Platform Notes (Continued)

0:  10  21
1:  21  10

From /proc/meminfo
MemTotal: 394864760 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-3joc 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 14 03:38

SPEC is set to: /home/cpu2017
    Filesystem  Type  Size  Used  Avail  Use% Mounted on
    /dev/sda3    xfs  516G  114G  403G  23%  /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
    Memory:
        24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPECrate2017_int_base = 66.6
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jun-2017

Compiler Version Notes

==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
   525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
CC   500.perlbench_r(peak) 502.gcc_r(peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
   541.leela_r(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
   541.leela_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
FC  548.exchange2_r(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
   icc

C++ benchmarks:
   icpc

(Continued on next page)
**SPEC CPU2017 Integer Rate Result**

Cisco Systems  
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)  

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<tr>
<th>SPECrate2017_int_base</th>
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**CPU2017 License:** 9019  
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**Software Availability:** Jun-2017  
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**Test Date:** Dec-2017

**Base Compiler Invocation (Continued)**

Fortran benchmarks:
ifort

**Base Portability Flags**

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-1hs -align array32byte  
-L/usr/local/je5.0.1-64/lib -ljemalloc

**Base Other Flags**

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPECrate2017_int_base = 66.6
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CPU2017 License: 9019
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Test Date: Dec-2017
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Software Availability: Jun-2017

Base Other Flags (Continued)

Fortran benchmarks:
- m64

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib
-ljemalloc

502.gcc_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Peak Optimization Flags (Continued)

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib
-ljemalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/usr/local/je5.0.1-64/lib -ljemalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-64/lib -ljemalloc

523.xalancbmk_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Other Flags

C benchmarks (except as noted below):
-m64 -std=c11

502.gcc_r: -m32 -std=c11

C++ benchmarks (except as noted below):
-m64

523.xalancbmk_r: -m32

(Continued on next page)
## Peak Other Flags (Continued)

Fortran benchmarks:
- m64

The flags files that were used to format this result can be browsed at:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)