## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6148, 2.40 GHz)

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

<table>
<thead>
<tr>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
</table>

### SPECspeed2017

- **SPECspeed2017_int_base = 9.02**
- **SPECspeed2017_int_peak = 9.27**

### Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed2017_int_base (9.02)</th>
<th>SPECspeed2017_int_peak (9.27)</th>
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<tbody>
<tr>
<td>perlbench_s</td>
<td>80</td>
<td>6.23</td>
<td>7.41</td>
</tr>
<tr>
<td>gcc_s</td>
<td>80</td>
<td>9.50</td>
<td>9.79</td>
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<tr>
<td>mcf_s</td>
<td>80</td>
<td>11.2</td>
<td>11.3</td>
</tr>
<tr>
<td>omnetpp_s</td>
<td>80</td>
<td>6.65</td>
<td>6.66</td>
</tr>
<tr>
<td>xalancbmk_s</td>
<td>80</td>
<td>9.55</td>
<td>10.1</td>
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<tr>
<td>x264_s</td>
<td>80</td>
<td>11.9</td>
<td>17.8</td>
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<tr>
<td>deepsjeng_s</td>
<td>80</td>
<td>5.06</td>
<td>5.03</td>
</tr>
<tr>
<td>leela_s</td>
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<td>4.35</td>
<td>4.36</td>
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<tr>
<td>exchange2_s</td>
<td>80</td>
<td>13.3</td>
<td>17.4</td>
</tr>
<tr>
<td>xz_s</td>
<td>80</td>
<td>24.3</td>
<td>24.3</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6148  
  **Max MHz.:** 3700  
  **Nominal:** 2400  
  **Enabled:** 80 cores, 4 chips  
  **Orderable:** 2,4 Chips  
  **Cache L1:** 32 KB I + 32 KB D on chip per core  
  **L2:** 1 MB I+D on chip per core  
  **L3:** 27.5 MB I+D on chip per chip  
  **Memory:** 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)  
  **Storage:** 1 x 600 GB SAS HDD, 10K RPM  
  **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)  
  **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++  
  **Fortran:** Version 18.0.0.128 of Intel Fortran  
  **Firmware:** Version 3.2.2a released Sep-2017  
  **File System:** xfs  
  **System State:** Run level 3 (multi-user)  
  **Base Pointers:** 64-bit  
  **Peak Pointers:** 32/64-bit  
  **Other:** jemalloc: jemalloc memory allocator library V5.0.1;  
  jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets;  
  jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;  
  jemalloc: sources available from jemalloc.net or releases
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
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<tr>
<td>600.perlbench_s</td>
<td>80</td>
<td>285</td>
<td>6.23</td>
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<td>80</td>
<td>245</td>
<td>6.65</td>
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<td>80</td>
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<td>255</td>
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<td>80</td>
<td>252</td>
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<td>255</td>
<td>24.2</td>
</tr>
</tbody>
</table>

SPECspeed2017_int_base = 9.02
SPECspeed2017_int_peak = 9.27

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64:/opt/cpu2017/je5.0.1-32:/opt/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
`sync; echo 3 > /proc/sys/vm/drop_caches`

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly

(Continued on next page)
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Cisco UCS B480 M5 (Intel Xeon Gold 6148, 2.40 GHz)

<table>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

**General Notes (Continued)**

generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

**Platform Notes**

**BIOS Settings:**  
Intel HyperThreading Technology set to Disabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Disabled  
Patrol Scrub set to Disabled  
Sysinfo program /opt/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
runtime on linux-qiwr Mon Nov 27 04:22:16 2017

**SUT (System Under Test) info as seen by some common utilities.**  
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name: Intel(R) Xeon(R) Gold 6148 CPU @ 2.40GHz
- 4 "physical id"s (chips)
- 80 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

- cpu cores : 20
- siblings : 20
- physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
- physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
- physical 2: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
- physical 3: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:

- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 80
- On-line CPU(s) list: 0-79
- Thread(s) per core: 1

(Continued on next page)
SPEC CPU2017 Integer Speed Result

Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECspeed2017_int_base = 9.02
SPECspeed2017_int_peak = 9.27

Platform Notes (Continued)

Core(s) per socket: 20
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6148 CPU @ 2.40GHz
Stepping: 4
CPU MHz: 1160.327
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39
NUMA node2 CPU(s): 40-59
NUMA node3 CPU(s): 60-79

Flags: fpu vme de pse mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl apic sm mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl apic sm mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl apic sm mtrr pge mca cmov

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

Available: 4 nodes (0-3)
Node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
Node 0 size: 191927 MB
Node 0 free: 191348 MB
Node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
Node 1 size: 193521 MB
Node 1 free: 192915 MB
Node 2 cpus: 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59
Node 2 size: 193521 MB
Node 2 free: 193028 MB

(Continued on next page)
SPEC CPU2017 Integer Speed Result

Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECspeed2017_int_base = 9.02
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CPU2017 License: 9019
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Test Date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

node 3 cpus: 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
node 3 size: 193518 MB
node 3 free: 192971 MB
node distances:
node 0 1 2 3
 0: 10 21 21 21
 1: 21 10 21 21
 2: 21 21 10 21
 3: 21 21 21 10

From /proc/meminfo
MemTotal: 791028648 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-qiwr 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 4 06:35

SPEC is set to: /opt/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 280G 144G 136G 52% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B480M5.3.2.2a.0.0919171641 09/19/2017
Memory:

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPEC CPU2017 Integer Speed Result
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SPECspeed2017_int_base = 9.02
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2017
Hardware Availability: Aug-2017
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Software Availability: Sep-2017

Platform Notes (Continued)

48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666
(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base, peak) 657.xz_s(base)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
CC 600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base) 641.leela_s(base)
==============================================================================
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
CXXC 620.omnetpp_s(peak) 623.xalancbmk_s(peak) 631.deepsjeng_s(peak) 641.leela_s(peak)
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
FC 648.exchange2_s(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECspeed2017_int_base = 9.02
SPECspeed2017_int_peak = 9.27

Base Compiler Invocation

C benchmarks:
- icc

C++ benchmarks:
- icpc

Fortran benchmarks:
- ifort

Base Portability Flags

600.perlbmk_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
- W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
- L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
- W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
- W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
- L/usr/local/je5.0.1-64/lib -ljemalloc
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECcpu2017 Integer Speed Result

Specspeed2017_int_base = 9.02
Specspeed2017_int_peak = 9.27

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2017
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Hardware Availability: Aug-2017
Software Availability: Sep-2017

Base Other Flags

C benchmarks:
- m64 -std=c11

C++ benchmarks:
- m64

Fortran benchmarks:
- m64

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

(Continued on next page)
Peak Optimization Flags (Continued)

600.perlbench_s (continued):
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

623.xalancbmk_s: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-32/lib -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6148, 2.40 GHz)

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<tr>
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**SPECspeed2017_int_base = 9.02**

**SPECspeed2017_int_peak = 9.27**

**Peak Other Flags**

C benchmarks:
- `-m64 -std=c11`

C++ benchmarks (except as noted below):
- `-m64`
  - `623.xalancbmk_s: -m32`

Fortran benchmarks:
- `-m64`

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
[http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

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