Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
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<tr>
<td>503.bwaves_r</td>
<td>104</td>
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<td>507.cactusBSSN_r</td>
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<td>549.fotonik3d_r</td>
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<tr>
<td>554.roms_r</td>
<td>104</td>
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</tr>
</tbody>
</table>

**Hardware**

- **CPU Name**: Intel Xeon Platinum 8164
- **Max MHz**: 3700
- **Nominal**: 2000
- **Enabled**: 52 cores, 2 chips, 2 threads/core
- **Orderable**: 1.2 Chips
- **Cache L1**: 32 KB I + 32 KB D on chip per core
- **Cache L2**: 1 MB I+D on chip per core
- **Cache L3**: 35.75 MB I+D on chip per chip
- **Memory**: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
- **Storage**: 1 x 1 TB SAS HDD, 10K RPM
- **Other**: None

**Software**

- **OS**: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default
- **Compiler**: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
- **Parallel**: No
- **Firmware**: Version 3.2.3c released Mar-2018
- **File System**: xfs
- **System State**: Run level 3 (multi-user)
- **Base Pointers**: 64-bit
- **Peak Pointers**: 64-bit
- **Other**: None
- **Power Management**: --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 227
SPECrate®2017_fp_peak = 228

**Results Table**

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</tr>
</tbody>
</table>

SPECrate®2017_fp_base = 227
SPECrate®2017_fp_peak = 228

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

**Submit Notes**

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor.

For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "~/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz) SPECrate®2017_fp_base = 227
SPECrate®2017_fp_peak = 228

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: May-2018
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Mar-2018

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-uezu Wed May 9 01:32:35 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8164 CPU @ 2.00GHz
  2 "physical id"s (chips)
  104 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 26
siblings : 52
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 104
On-line CPU(s) list: 0-103
Thread(s) per core: 2
Core(s) per socket: 26
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |

| Test Date: | May-2018 |
| Hardware Availability: | Aug-2017 |
| Software Availability: | Mar-2018 |

### Platform Notes (Continued)

- Model: 85
- Model name: Intel(R) Xeon(R) Platinum 8164 CPU @ 2.00GHz
- Stepping: 4
- CPU MHz: 2565.466
- CPU max MHz: 3700.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 4000.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 36608K
- NUMA node0 CPU(s): 0-3,7-9,13-15,20-22,52-55,59-61,65-67,72-74
- NUMA node1 CPU(s): 4-6,10-12,16-19,23-25,56-58,62-64,68-71,75-77
- NUMA node2 CPU(s): 26-29,33-35,39-41,46-48,78-81,85-87,91-93,98-100
- NUMA node3 CPU(s): 30-32,36-38,42-45,49-51,82-84,88-90,94-97,101-103
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpre pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bm1 hle avx2 smep bmi2 erts invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavefc xgetbv1 cqm_11c cqm_occip_11c

```
From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 7 8 9 13 14 15 20 21 22 52 53 54 55 59 60 61 65 66 67 72 73 74
  node 0 size: 95320 MB
  node 0 free: 95152 MB
  node 1 cpus: 4 5 6 10 11 12 16 17 18 19 23 24 25 56 57 58 62 63 64 68 69 70 71 75 76 77
  node 1 size: 96753 MB
  node 1 free: 96500 MB
  node 2 cpus: 26 27 28 29 33 34 35 39 40 41 46 47 48 78 79 80 81 85 86 87 91 92 93 98 99
  node 2 size: 96753 MB
  node 2 free: 96326 MB
  node 3 cpus: 30 31 32 36 37 38 42 43 44 45 49 50 51 82 83 84 88 90 94 95 96 97 101
  node 3 size: 96750 MB
  node 3 free: 95661 MB
```

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_fp_base = 227
SPECrate®2017_fp_peak = 228

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: May-2018
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

node distances:
node  0  1  2  3
0:  10 11 21 21
1:  11 10 21 21
2:  21 21 10 11
3:  21 21 11 10

From /proc/meminfo
MemTotal:       394831664 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-uezu 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 28 21:11

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used  Avail Use% Mounted on
  /dev/sda1    xfs  894G  364G  531G  41%  /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.3.2.3c.0.0307181316 03/07/2018
  Memory:
  24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

Test Sponsor: Cisco Systems
Hardware Availability: Aug-2017
Test Date: May-2018
Software Availability: Mar-2018

CPU2017 License: 9019
Tested by: Cisco Systems

Compiler Version Notes

C
  519.lbm_r(base, peak) 538.imagick_r(base, peak)
  544.nab_r(base, peak)

icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

C++
  508.namd_r(base, peak) 510.parest_r(base, peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

C++, C
  511.povray_r(base, peak) 526.blender_r(base, peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

C++, C, Fortran
  507.cactuBSSN_r(base, peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Fortran
  503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
  554.roms_r(base, peak)

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Fortran, C
  521.wrf_r(base, peak) 527.cam4_r(base, peak)

ifort (IFORT) 18.0.2 20180210

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrater®2017_fp_base = 227
SPECrater®2017_fp_peak = 228

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Copyright 2017-2019 Standard Performance Evaluation Corporation

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -fununsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Compiler Version Notes (Continued)

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_fp_base = 227
SPECrate®2017_fp_peak = 228

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

SPECrate®2017_fp_base = 227
SPECrate®2017_fp_peak = 228

CPU2017 License: 9019
Test Date: May-2018
Test Sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Mar-2018

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -03
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

538.imagick_r: -xCORE-AVX2 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

544.nab_r: Same as 519.lbm_r

C++ benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -03
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:
503.bwaves_r: -xCORE-AVX2 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -03
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -03
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -03
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8164, 2.00 GHz)

Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:
- prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
- no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml