## SPEC CPU®2017 Integer Speed Result

### Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6144, 3.50 GHz)

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>May-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2018</td>
</tr>
</tbody>
</table>

### CPU2017 License:
9019

### Test Sponsor:
Cisco Systems

### Tested by:
Cisco Systems

### Test Date:
May-2018

Common threads: 16

| SPECspeed®2017_int_base = 9.69 | SPECspeed®2017_int_peak = 9.94 |

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_s</td>
<td>6.97</td>
<td>8.12</td>
</tr>
<tr>
<td>gcc_s</td>
<td>9.69</td>
<td>10.3</td>
</tr>
<tr>
<td>mcf_s</td>
<td>12.1</td>
<td>12.2</td>
</tr>
<tr>
<td>omnetpp_s</td>
<td>6.80</td>
<td>6.95</td>
</tr>
<tr>
<td>xalancbmk_s</td>
<td>10.6</td>
<td>11.4</td>
</tr>
<tr>
<td>x264_s</td>
<td>12.0</td>
<td>12.0</td>
</tr>
<tr>
<td>deepsjeng_s</td>
<td>5.74</td>
<td>5.59</td>
</tr>
<tr>
<td>leela_s</td>
<td>4.96</td>
<td>4.96</td>
</tr>
<tr>
<td>exchange2_s</td>
<td>15.0</td>
<td>15.1</td>
</tr>
<tr>
<td>xz_s</td>
<td>22.3</td>
<td>22.4</td>
</tr>
</tbody>
</table>

---

### Hardware
- **CPU Name:** Intel Xeon Gold 6144
- **Max MHz:** 4200
- **Nominal:** 3500
- **Enabled:** 16 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 24.75 MB I+D on chip per chip
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 240 GB M.2 SATA SSD
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default
- **Compiler:** C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.2.3c released Mar-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc: jemalloc memory allocator library V5.0.1;
- **Power Management:** --
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>16</td>
<td>253</td>
<td>7.01</td>
<td>255</td>
<td>6.97</td>
<td>254</td>
<td>6.97</td>
<td>16</td>
<td>219</td>
<td>8.12</td>
<td>215</td>
<td>8.25</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>16</td>
<td>381</td>
<td>10.5</td>
<td>386</td>
<td>10.3</td>
<td>388</td>
<td>10.3</td>
<td>16</td>
<td>381</td>
<td>10.5</td>
<td>377</td>
<td>10.6</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>16</td>
<td>386</td>
<td>10.5</td>
<td>386</td>
<td>10.5</td>
<td>385</td>
<td>10.3</td>
<td>16</td>
<td>389</td>
<td>12.1</td>
<td>386</td>
<td>12.2</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>16</td>
<td>229</td>
<td>7.11</td>
<td>232</td>
<td>7.03</td>
<td>235</td>
<td>6.95</td>
<td>16</td>
<td>232</td>
<td>7.03</td>
<td>235</td>
<td>6.95</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>16</td>
<td>133</td>
<td>10.6</td>
<td>134</td>
<td>10.5</td>
<td>133</td>
<td>10.6</td>
<td>16</td>
<td>125</td>
<td>11.4</td>
<td>125</td>
<td>11.4</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>16</td>
<td>147</td>
<td>12.0</td>
<td>147</td>
<td>12.0</td>
<td>147</td>
<td>12.0</td>
<td>16</td>
<td>147</td>
<td>12.0</td>
<td>147</td>
<td>12.0</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>16</td>
<td>250</td>
<td>5.74</td>
<td>250</td>
<td>5.74</td>
<td>250</td>
<td>5.74</td>
<td>16</td>
<td>252</td>
<td>5.69</td>
<td>252</td>
<td>5.69</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>16</td>
<td>344</td>
<td>4.95</td>
<td>344</td>
<td>4.96</td>
<td>344</td>
<td>4.96</td>
<td>16</td>
<td>344</td>
<td>4.96</td>
<td>345</td>
<td>4.95</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>16</td>
<td>196</td>
<td>15.0</td>
<td>195</td>
<td>15.1</td>
<td>195</td>
<td>15.1</td>
<td>16</td>
<td>195</td>
<td>15.0</td>
<td>196</td>
<td>15.0</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>16</td>
<td>280</td>
<td>22.1</td>
<td>278</td>
<td>22.3</td>
<td>277</td>
<td>22.3</td>
<td>16</td>
<td>275</td>
<td>22.4</td>
<td>276</td>
<td>22.4</td>
</tr>
</tbody>
</table>

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### General Notes

Environment variables set by runcpu before the start of the run:

```
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"
```

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Files system page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets;

jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;

jemalloc: sources available from jemalloc.net or

---

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6144, 3.50 GHz)

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

SPECspeed®2017_int_base = 9.69
SPECspeed®2017_int_peak = 9.94

Test Date: May-2018  
Hardware Availability: Aug-2017
Software Availability: Mar-2018

General Notes (Continued)


Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-mys2 Mon May 21 20:32:16 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Gold 6144 CPU @ 3.50GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 8
siblings: 8
physical 0: cores 0 2 3 9 16 19 26 27
physical 1: cores 0 2 3 9 16 19 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6144 CPU @ 3.50GHz
Stepping: 4
CPU MHz: 1520.073
CPU max MHz: 4200.0000

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6144, 3.50 GHz)

SPECspeed®2017_int_base = 9.69
SPECspeed®2017_int_peak = 9.94

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

CPU min MHz: 1200.0000
BogoMIPS: 6999.99
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pmse pxdpm sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc
artic arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpref eagerfpup mni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2
ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 ssse2 sse4_2 x2apic movbe
popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch
ida arat epb invpcid_single pln pts dtherm hwlp_hwp_act_window
hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow
vnumi fexpriority ept vpid fsqosbase tsc_adjust bmi1 hle avx2 smep bmi2
erns invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm _llc cqm _occup _llc

/proc/cpuinfo cache data
    cache size: 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5 6 7
    node 0 size: 192074 MB
    node 0 free: 191717 MB
    node 1 cpus: 8 9 10 11 12 13 14 15
    node 1 size: 193504 MB
    node 1 free: 193202 MB
    node distances:
        node 0 1
        0: 10 21
        1: 21 10

From /proc/meminfo
    MemTotal: 394832560 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
    SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
    SuSE-release:

(Continued on next page)
# SPEC CPU®2017 Integer Speed Result

## Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6144, 3.50 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base = 9.69</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak = 9.94</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>May-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Mar-2018</td>
</tr>
</tbody>
</table>

### Platform Notes (Continued)

```
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:
Linux linux-mys2 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Dec 31 21:21
```

```
SPEC is set to: /home/cpu2017
```

```
Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda3      xfs   182G   46G  137G  26% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. B200M5.3.2.3c.0.0307181316 03/07/2018
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666
```

(End of data from sysinfo program)

### Compiler Version Notes

```
==============================================================================
C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
| 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
```

```
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

```
==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6144, 3.50 GHz)

<table>
<thead>
<tr>
<th>SPEC CPU®2017_int_base</th>
<th>9.69</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPEC CPU®2017_int_peak</td>
<td>9.94</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>631.deepsjeng_s(base, peak) 641.leela_s(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>icpc (ICC) 18.0.2 20180210</td>
</tr>
<tr>
<td>Copyright (C) 1985-2018 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fortran</th>
<th>648.exchange2_s(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ifort (IFORT) 18.0.2 20180210</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2018 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6144, 3.50 GHz)

SPEC CPU®2017 Integer Speed Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECspeed®2017_int_base = 9.69
SPECspeed®2017_int_peak = 9.94

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Base Optimization Flags (Continued)

C benchmarks (continued):
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64

623.xalancbmk_s: icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32

Fortran benchmarks:
ifort -m64

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6144, 3.50 GHz)

SPEC\textsuperscript{CPU}\textsuperscript{\textregistered}2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

SPECspeed\textsuperscript{\textregistered}2017\_int\_base = 9.69
SPECspeed\textsuperscript{\textregistered}2017\_int\_peak = 9.94

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Peak Optimization Flags

C benchmarks:

600.perlbench\(_s\): \texttt{-Wl,-z,muldefs \-prof-gen(pass 1) \-prof-use(pass 2) \-O2}
-xCORE-AVX512 \-qopt-mem-layout-trans=3 \-ipo \-O3
-no-prec-div \-DSPEC\_SUPPRESS\_OPENMP \-qopenmp
-DSPEC\_OPENMP \-fno-strict-overflow
-L/home/cpu2017/je5.0.1-64/ \-ljemalloc

602.gcc\(_s\): \texttt{-Wl,-z,muldefs \-prof-gen(pass 1) \-prof-use(pass 2) \-O2}
-xCORE-AVX512 \-qopt-mem-layout-trans=3 \-ipo \-O3
-no-prec-div \-DSPEC\_SUPPRESS\_OPENMP \-qopenmp
-DSPEC\_OPENMP \-L/home/cpu2017/je5.0.1-64/ \-ljemalloc

605.mcf\(_s\): \texttt{-Wl,-z,muldefs \-prof-gen(pass 1) \-prof-use(pass 2) \-ipo}
-xCORE-AVX512 \-O3 \-no-prec-div \-qopt-mem-layout-trans=3
-DSPEC\_SUPPRESS\_OPENMP \-qopenmp \-DSPEC\_OPENMP
-L/home/cpu2017/je5.0.1-64/ \-ljemalloc

625.x264\(_s\): \texttt{-Wl,-z,muldefs \-xCORE-AVX512 \-ipo \-O3 \-no-prec-div}
-qopt-mem-layout-trans=3 \-qopenmp \-DSPEC\_OPENMP
-L/home/cpu2017/je5.0.1-64/ \-ljemalloc

657.xz\(_s\): Same as 602.gcc\(_s\)

C++ benchmarks:

620.omnetpp\(_s\): \texttt{-Wl,-z,muldefs \-prof-gen(pass 1) \-prof-use(pass 2) \-ipo}
-xCORE-AVX512 \-O3 \-no-prec-div \-qopt-mem-layout-trans=3
-DSPEC\_SUPPRESS\_OPENMP \-qopenmp \-DSPEC\_OPENMP
-L/home/cpu2017/je5.0.1-64/ \-ljemalloc

623.xalancbmk\(_s\): \texttt{-Wl,-z,muldefs \-prof-gen(pass 1) \-prof-use(pass 2) \-ipo}
-xCORE-AVX512 \-O3 \-no-prec-div \-qopt-mem-layout-trans=3
-DSPEC\_SUPPRESS\_OPENMP \-qopenmp \-DSPEC\_OPENMP
-L/home/cpu2017/je5.0.1-32/ \-ljemalloc

631.deepsjeng\(_s\): Same as 620.omnetpp\(_s\)

641.leelu\(_s\): Same as 620.omnetpp\(_s\)

Fortran benchmarks:

\texttt{-Wl,-z,muldefs \-xCORE-AVX512 \-ipo \-O3 \-no-prec-div}
-qopt-mem-layout-trans=3 \-nostandard-realloc-lhs \-align array32byte
-L/home/cpu2017/je5.0.1-64/ \-ljemalloc
## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Gold 6144, 3.50 GHz)  

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>9.69</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
<td>9.94</td>
</tr>
</tbody>
</table>

### Details:

- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Tested by:** Cisco Systems
- **Test Date:** May-2018
- **Hardware Availability:** Aug-2017
- **Software Availability:** Mar-2018

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


---

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-05-21 23:32:15-0400.  
Originally published on 2018-06-12.