Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECspeed®2017_fp_base = 119</th>
<th>SPECspeed®2017_fp_peak = 120</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License:</td>
<td>9019</td>
<td>Test Date:</td>
</tr>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
</tr>
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<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
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<table>
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<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base (119)</th>
<th>SPECspeed®2017_fp_peak (120)</th>
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</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>48</td>
<td>168</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>48</td>
<td>171</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>48</td>
<td>43.9</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>48</td>
<td>85.3</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>48</td>
<td>92.8</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>48</td>
<td>57.1</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>48</td>
<td>118</td>
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<tr>
<td>644.nab_s</td>
<td>48</td>
<td>241</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>48</td>
<td>149</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>48</td>
<td>152</td>
</tr>
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<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
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</thead>
<tbody>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Platinum 8160M</td>
</tr>
<tr>
<td>Max MHz:</td>
<td>3700</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2100</td>
</tr>
<tr>
<td>Enabled:</td>
<td>48 cores, 2 chips</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
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<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
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<tr>
<td>L3:</td>
<td>33 MB I+D on chip per chip</td>
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<td>Memory:</td>
<td>384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)</td>
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<td>Storage:</td>
<td>1 x 1 TB SAS HDD, 7.2K RPM</td>
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<tr>
<td>Other:</td>
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<td>OS:</td>
<td>SUSE Linux Enterprise Server 12 SP2 (x86_64)</td>
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<td>4.4.103-92.56-default</td>
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<td>Compiler:</td>
<td>C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux</td>
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<td>Parallel:</td>
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<td>Firmware:</td>
<td>Version 3.2.3c released Mar-2018</td>
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<td>File System:</td>
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<td>System State:</td>
<td>Run level 3 (multi-user)</td>
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<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
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<tr>
<td>Peak Pointers:</td>
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<td>Other:</td>
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<td>Power Management:</td>
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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<tr>
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>171</td>
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<td>117</td>
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<td>152</td>
<td>106</td>
<td>149</td>
<td>102</td>
<td>155</td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 119
SPECspeed®2017_fp_peak = 120

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

SPECspeed®2017_fp_base = 119
SPECspeed®2017_fp_peak = 120

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b0c91c0f
running on linux-uezu Sun Jun 3 01:27:42 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name: Intel(R) Xeon(R) Platinum 8160M CPU @ 2.10GHz
        2 "physical id"s (chips)
        48 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
        cpu cores : 24
        siblings : 24
        physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
        physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

From lscpu:
    Architecture: x86_64
    CPU op-mode(s): 32-bit, 64-bit
    Byte Order: Little Endian
    CPU(s): 48
    On-line CPU(s) list: 0-47
    Thread(s) per core: 1
    Core(s) per socket: 24
    Socket(s): 2
    NUMA node(s): 2
    Vendor ID: GenuineIntel
    CPU family: 6
    Model: 85
    Model name: Intel(R) Xeon(R) Platinum 8160M CPU @ 2.10GHz
    Stepping: 4
    CPU MHz: 3603.028
    CPU max MHz: 3700.0000
    CPU min MHz: 1000.0000
    BogoMIPS: 4200.01
    Virtualization: VT-x
    L1d cache: 32K
    L1i cache: 32K
    L2 cache: 1024K
    L3 cache: 33792K

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

| SPECspeed®2017_fp_base = 119 |
| SPECspeed®2017_fp_peak = 120 |

**CPU2017 License:** 9019
**Test Date:** Jun-2018
**Test Sponsor:** Cisco Systems
**Hardware Availability:** Aug-2017
**Tested by:** Cisco Systems
**Software Availability:** Mar-2018

### Platform Notes (Continued)

NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
Flags: fpu vme de tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good ntopology nonstop_tsc
aperfmon perf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb invpcид Single p1n pts
dtherm hwlp hwlp_act_window hwlp_epp hwlp_req intel_pt spec_ctrl kaiser tpr_shadow
vmx flexpriority ept vpd fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid
rtn cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw
avx512vl xsavesopt xsavex xgetbv1 cqm_llc cqm_occup_llc

```
From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.

Node 0: cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
          size: 192074 MB
          free: 188266 MB

Node 1: cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
          size: 193504 MB
          free: 189573 MB

Node distances:
  0:  10  21
  1:  21  10
```

```
From /proc/meminfo
MemTotal:       394832424 kB
MemAvailable:   386801820 kB
MemFairness:    0
MemFree:        16020604 kB
MemSwap:        0 kB
MemInit:        0 kB
MemCommit:      0 kB
MemShared:      0 kB
HugePages_Total:       0
HugePages_Free:        0
HugePages_Rsvd:        0
HugePages_Rsvnm:       0
Hugepagesize:       2048 kB
```

```
From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECspeed®2017_fp_base = 119
SPECspeed®2017_fp_peak = 120

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Hardware Availability: Aug-2017
Test Date: Jun-2018
Software Availability: Mar-2018
Tested by: Cisco Systems

Platform Notes (Continued)

ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
 Linux linux-uezu 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jun 2 23:32
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 894G 111G 784G 13% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.3c.0.0307181316 03/07/2018
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak) |
| C               | 644.nab_s(base, peak) |
==============================================================================
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================
| C++, C, Fortran | 607.cactuBSSN_s(base, peak) |
==============================================================================
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

SPECspeed®2017_fp_base = 119
SPECspeed®2017_fp_peak = 120

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jun-2018
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Compiler Version Notes (Continued)

Fortran
603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
654.roms_s(base, peak)

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Fortran, C
621.wrf_s(base, peak) 627.cam4_s(base, peak)
628.pop2_s(base, peak)

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64

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SPECspeed®2017_fp_base = 119
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Test Date: Jun-2018
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**Base Portability Flags (Continued)**

654.roms_s: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

**Peak Compiler Invocation**

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

SPECspeed®2017_fp_base = 119
SPECspeed®2017_fp_peak = 120

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch
-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

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Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-06-03 01:27:41-0400.