## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS B480 M5 (Intel Xeon Gold 5120, 2.20 GHz)

<table>
<thead>
<tr>
<th>threads</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.hwaves_s</td>
<td>156</td>
<td>156</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>70.5</td>
<td>70.5</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>63.0</td>
<td>63.0</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>64.9</td>
<td>64.9</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>88.2</td>
<td>89.4</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>24.3</td>
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</tr>
<tr>
<td>638.imagick_s</td>
<td>131</td>
<td>131</td>
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<tr>
<td>644.nab_s</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>95.4</td>
<td>95.2</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>165</td>
<td>165</td>
</tr>
</tbody>
</table>

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default
- **Compiler:** C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.2.3c released Mar-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --

### Hardware

- **CPU Name:** Intel Xeon Gold 5120
- **Max MHz:** 3200
- **Nominal:** 2200
- **Enabled:** 56 cores, 4 chips
- **Orderable:** 2.4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 19.25 MB I+D on chip per chip
- **Memory:** 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Storage:** 1 x 240 GB M.2 SATA SSD
- **Other:** None

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Cisco Systems

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Cisco UCS B480 M5 (Intel Xeon Gold 5120, 2.20 GHz)

| Threads | 0  | 30.0 | 70.0 | 100 | 130 | 160 | 190 | 220 | 250 | 280 | 310 | 340 | 370 | 400 | 430 | 460 | 490 | 520 | 550 | 580 | 610 | 640 | 670 | 700 | 730 |
|---------|----|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 603.hwaves_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 607.cactuBSSN_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 619.lbm_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 621.wrf_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 627.cam4_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 628.pop2_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 638.imagick_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 644.nab_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 649.fotonik3d_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 654.roms_s | 56 |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

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SPEC CPU®2017 License: 9019 Test Date: Jun-2018

Test Sponsor: Cisco Systems Hardware Availability: Aug-2017

Tested by: Cisco Systems Software Availability: Mar-2018
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 5120, 2.20 GHz)

SPECspeed®2017_fp_base = 118
SPECspeed®2017_fp_peak = 120

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Seconds</th>
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<th>Seconds</th>
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<tbody>
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<td>96.0</td>
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<td>56</td>
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<td>170</td>
<td>91.6</td>
<td>172</td>
<td>93.3</td>
<td>169</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled

(Continued on next page)
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Cisco UCS B480 M5 (Intel Xeon Gold 5120, 2.20 GHz)

SPECspeed®2017_fp_base = 118
SPECspeed®2017_fp_peak = 120

Platform Notes (Continued)

CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bdc091c0f
running on linux-xy4f Thu Jun 7 07:20:01 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5120 CPU @ 2.20GHz
4 "physical id"s (chips)
56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 14
siblings : 14
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 56
On-line CPU(s) list: 0-55
Thread(s) per core: 1
Core(s) per socket: 14
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5120 CPU @ 2.20GHz
Stepping: 4
CPU MHz: 1000.108
CPU max MHz: 3200.000
CPU min MHz: 1000.000
BogoMIPS: 4399.99
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
Cisco Systems  
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SPECspeed®2017_fp_base = 118  
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CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Test Date: Jun-2018  
Hardware Availability: Aug-2017  
Tested by: Cisco Systems  
Software Availability: Mar-2018

Platform Notes (Continued)

L2 cache: 1024K  
L3 cache: 19712K  
NUMA node0 CPU(s): 0-13  
NUMA node1 CPU(s): 14-27  
NUMA node2 CPU(s): 28-41  
NUMA node3 CPU(s): 42-55  
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpupi pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpmr pdcmtscid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invvpid_single pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow vmni flexpriority ept vpid fsgbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsavesopt xsavec xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data  
cache size : 19712 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.  
available: 4 nodes (0-3)  
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13  
node 0 size: 192088 MB  
node 0 free: 190893 MB  
node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27  
node 1 size: 193521 MB  
node 1 free: 192117 MB  
node 2 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41  
node 2 size: 193521 MB  
node 2 free: 190726 MB  
node 3 cpus: 42 43 44 45 46 47 48 49 50 51 52 53 54 55  
node 3 size: 193518 MB  
node 3 free: 190837 MB

node distances:  
0: 10 21 31 21  
1: 21 10 21 31  
2: 31 21 10 21  
3: 21 31 21 10

From /proc/meminfo  
MemTotal: 791193292 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB

(Continued on next page)
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Platform Notes (Continued)

From /etc/*release* /etc/*version*

SuSE-release:
  - SUSE Linux Enterprise Server 12 (x86_64)
  - VERSION = 12
  - PATCHLEVEL = 2

# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

os-release:
  - NAME="SLES"
  - VERSION="12-SP2"
  - VERSION_ID="12.2"
  - PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  - ID="sles"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  - Linux linux-xy4f 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
  - x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 3 05:01

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda1      xfs   224G   74G  150G  34% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
Memory:
  - 48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base, peak)</th>
</tr>
</thead>
</table>
==============================================================================
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
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Compiler Version Notes (Continued)

C++, C, Fortran | 607.cactuBSSN_s(base, peak)
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
| 628.pop2_s(base, peak)
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64
## Cisco Systems
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### CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

### Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

### Base Portability Flags
- 603.bwaves_s: -DSPEC_LP64
- 607.cactuBSSN_s: -DSPEC_LP64
- 619.lbm_s: -DSPEC_LP64
- 621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
- 638.imagick_s: -DSPEC_LP64
- 644.nab_s: -DSPEC_LP64
- 649.fotonik3d_s: -DSPEC_LP64
- 654.roms_s: -DSPEC_LP64

### Base Optimization Flags

#### C benchmarks:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

#### Fortran benchmarks:
- -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
- -nostandard-realloc-lhs -align array32byte

#### Benchmarks using both Fortran and C:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
- -nostandard-realloc-lhs -align array32byte

#### Benchmarks using Fortran, C, and C++:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
- -nostandard-realloc-lhs -align array32byte

### Peak Compiler Invocation

#### C benchmarks:
icc -m64 -std=c11

#### Fortran benchmarks:
ifort -m64

(Continued on next page)
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:
prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

(Continued on next page)
## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 5120, 2.20 GHz)

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<td>Cisco Systems</td>
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### SPEC CPU 2017 Floating Point Speed Result

**SPECspeed**

- **SPECspeed®2017_fp_base = 118**
- **SPECspeed®2017_fp_peak = 120**

### Peak Optimization Flags (Continued)

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:

- `-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch`
- `-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3`
- `-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`
- `-align array32byte`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-06-07 07:20:00-0400.
