Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60 GHz)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 56.2
SPECrate®2017_int_peak = 59.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
CPU Name: Intel Xeon Platinum 8156
Max MHz: 3700
Nominal: 3600
Enabled: 8 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 16.5 MB I+D on chip per chip
Other: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default
Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 3.2.3c released Mar-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc: jemalloc memory allocator library V5.0.1;
Power Management: --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60 GHz)

SPECrate®2017_int_base = 56.2
SPECrate®2017_int_peak = 59.5

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>16</td>
<td>590</td>
<td>43.2</td>
<td>600</td>
<td>42.5</td>
<td>595</td>
<td>42.8</td>
<td>16</td>
<td>496</td>
<td>51.4</td>
<td>495</td>
<td>51.4</td>
<td>495</td>
<td>51.5</td>
</tr>
<tr>
<td>gcc_r</td>
<td>16</td>
<td>458</td>
<td>49.4</td>
<td>457</td>
<td>49.6</td>
<td>457</td>
<td>49.6</td>
<td>16</td>
<td>388</td>
<td>58.4</td>
<td>387</td>
<td>58.5</td>
<td>389</td>
<td>58.3</td>
</tr>
<tr>
<td>mcf_r</td>
<td>16</td>
<td>369</td>
<td>70.0</td>
<td>368</td>
<td>70.2</td>
<td>381</td>
<td>67.8</td>
<td>16</td>
<td>368</td>
<td>70.3</td>
<td>384</td>
<td>67.4</td>
<td>374</td>
<td>69.2</td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>16</td>
<td>615</td>
<td>34.1</td>
<td>618</td>
<td>34.0</td>
<td>616</td>
<td>34.1</td>
<td>16</td>
<td>618</td>
<td>34.0</td>
<td>617</td>
<td>34.0</td>
<td>618</td>
<td>33.9</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>16</td>
<td>274</td>
<td>61.7</td>
<td>277</td>
<td>60.9</td>
<td>278</td>
<td>60.9</td>
<td>16</td>
<td>233</td>
<td>72.6</td>
<td>233</td>
<td>72.6</td>
<td>233</td>
<td>72.4</td>
</tr>
<tr>
<td>x264_r</td>
<td>16</td>
<td>244</td>
<td>155</td>
<td>244</td>
<td>155</td>
<td>245</td>
<td>114</td>
<td>16</td>
<td>233</td>
<td>120</td>
<td>234</td>
<td>120</td>
<td>233</td>
<td>120</td>
</tr>
<tr>
<td>xz_r</td>
<td>16</td>
<td>435</td>
<td>39.7</td>
<td>435</td>
<td>39.7</td>
<td>435</td>
<td>39.7</td>
<td>16</td>
<td>435</td>
<td>39.7</td>
<td>436</td>
<td>39.7</td>
<td>435</td>
<td>39.7</td>
</tr>
</tbody>
</table>
| SPECrate®2017_int_base = 56.2
| SPECrate®2017_int_peak = 59.5

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc: configured and built at default for

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60 GHz)

General Notes (Continued)

32bit (i686) and 64bit (x86_64) targets;
jemalloc: built with the RedHat Enterprise 7.4,
and the system compiler gcc 4.8.5;
jemalloc: sources available from jemalloc.net or

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-qc7k Wed Jun 6 07:53:50 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8156 CPU @ 3.60GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 8
physical 0: cores 1 5 9 13
physical 1: cores 1 5 9 13

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 2
Core(s) per socket: 4
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60 GHz)

| SPECrate®2017_int_base = 56.2 |
|-------------------|-------------------|
| SPECrate®2017_int_peak = 59.5 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

| Model: | 85 |
| Model name: | Intel(R) Xeon(R) Platinum 8156 CPU @ 3.60GHz |
| Stepping: | 4 |
| CPU MHz: | 3700.000 |
| CPU max MHz: | 3700.0000 |
| CPU min MHz: | 1200.0000 |
| BogoMIPS: | 7200.03 |
| Virtualization: | VT-x |
| L1d cache: | 32K |
| L1i cache: | 32K |
| L2 cache: | 1024K |
| L3 cache: | 16896K |
| NUMA node0 CPU(s): | 0-3,8-11 |
| NUMA node1 CPU(s): | 4-7,12-15 |
| Flags: | fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt pнии sse4_1 sse4a2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epbi invpcid_single pti dtes60 hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3rms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_11c cqm_occup_llc |

/cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 8 9 10 11
    node 0 size: 192074 MB
    node 0 free: 191691 MB
    node 1 cpus: 4 5 6 7 12 13 14 15
    node 1 size: 193504 MB
    node 1 free: 193161 MB

    node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo

| MemTotal: | 394832552 kB |
| HugePages_Total: | 0 |
| Hugepagesize: | 2048 kB |
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60 GHz)

SPECrate®2017_int_base = 56.2
SPECrate®2017_int_peak = 59.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

From /etc/*release* /etc/*version*
SuSE-release:
   SUSE Linux Enterprise Server 12 (x86_64)
   VERSION = 12
   PATCHLEVEL = 2
   # This file is deprecated and will be removed in a future service pack or release.
   # Please check /etc/os-release for details about this release.
   os-release:
      NAME="SLES"
      VERSION="12-SP2"
      VERSION_ID="12.2"
      PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
      ID="sles"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-qc7k 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 1 10:59

SPEC is set to: /home/cpu2017
   Filesystem   Type  Size  Used Avail Use% Mounted on
   /dev/sda1      xfs   224G   64G  160G  29% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. B200M5.3.2.3c.0.0307181316 03/07/2018
   Memory:
      24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C     | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak) |
==============================================================================

icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60 GHz)  

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Jun-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Mar-2018</td>
</tr>
</tbody>
</table>

**SPECrated2017_int_base = 56.2**  
**SPECrated2017_int_peak = 59.5**

---

### Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>C++</th>
<th>520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>icpc (ICC)</td>
<td>18.0.2 20180210</td>
</tr>
<tr>
<td>Copyright (C) 1985–2018 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fortran</th>
<th>548.exchange2_r(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ifort (IFORT)</td>
<td>18.0.2 20180210</td>
</tr>
<tr>
<td>Copyright (C) 1985–2018 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

---

### Base Compiler Invocation

**C benchmarks:**  
```  
icc -m64 -std=c11  
```

**C++ benchmarks:**  
```  
icpc -m64  
```

**Fortran benchmarks:**  
```  
ifort -m64  
```

---

### Base Portability Flags

```  
500.perlbench_r -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r -DSPEC_LP64  
505.mcf_r -DSPEC_LP64  
520.omnetpp_r -DSPEC_LP64  
523.xalancbmk_r -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r -DSPEC_LP64  
531.deepsjeng_r -DSPEC_LP64  
541.leela_r -DSPEC_LP64  
548.exchange2_r -DSPEC_LP64  
557.xz_r -DSPEC_LP64  
```
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60 GHz)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 56.2
SPECrate®2017_int_peak = 59.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Base Optimization Flags

C benchmarks:
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

C++ benchmarks:
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

Fortran benchmarks:
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
- L/home/cpu2017/je5.0.1-64/ -ljemalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11
502.gcc_r: icc -m32 -std=c11 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32

C++ benchmarks (except as noted below):
icpc -m64
523.xalancbmk_r: icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60 GHz)

SPECrate®2017_int_peak = 59.5
SPECrate®2017_int_base = 56.2

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -o3 -no-prec-div -qopt-mem-layout-trans=3 -fno-strict-overflow -L/home/cpu2017/je5.0.1-64/ -ljemalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -o3 -no-prec-div -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-32/ -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -o3 -no-prec-div -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -o3 -no-prec-div -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at
### SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>Cisco Systems</th>
<th>SPECrate®2017_int_base = 56.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco UCS B200 M5 (Intel Xeon Platinum 8156, 3.60 GHz)</td>
<td>SPECrate®2017_int_peak = 59.5</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jun-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

You can also download the XML flags sources by saving the following links:


---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-06-06 07:53:49-0400.  