NEC Corporation

Express5800/R120h-2E (Intel Xeon Silver 4108)

SPECrates2017_fp_base = 81.7
SPECrates2017_fp_peak = 83.9

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Hardware
- CPU Name: Intel Xeon Silver 4108
- Max MHz.: 3000
- Nominal: 1800
- Enabled: 16 cores, 2 chips, 2 threads/core
- Orderable: 1.2 chips
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 11 MB I+D on chip per chip
- Other: None
- Memory: 192 GB (12 x 16 GB 2Rx8 PC4-2666V-R, running at 2400)
- Storage: 1 x 600 GB SAS, 15000 RPM, RAID 0
- Other: None

Software
- OS: Red Hat Enterprise Linux Server release 7.4 (Maipo)
- Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
- Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
- Parallel: No
- Firmware: NEC BIOS Version U31 02/14/2018 released Mar-2018
- File System: ext4
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: 64-bit
- Other: None
SPEC CPU2017 Floating Point Rate Result

NEC Corporation

Express5800/R120h-2E (Intel Xeon Silver 4108)

SPECrate2017_fp_base = 81.7
SPECrate2017_fp_peak = 83.9

Results Table

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<td>97.0</td>
<td>1281</td>
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<td>97.3</td>
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<td>1028</td>
<td>49.4</td>
<td>1025</td>
<td>49.6</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)
**SPEC CPU2017 Floating Point Rate Result**

**NEC Corporation**

Express5800/R120h-2E (Intel Xeon Silver 4108)

<table>
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<td>NEC Corporation</td>
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<tr>
<td>Tested by:</td>
<td>NEC Corporation</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Jul-2018</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Nov-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2018</td>
</tr>
</tbody>
</table>

**General Notes (Continued)**

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

**Platform Notes**

BIOS Settings:
- Thermal Configuration: Maximum Cooling
- Workload Profile: General Throughput Compute
- Memory Patrol Scrubbing: Disabled
- LLC Dead Line Allocation: Disabled
- LLC Prefetch: Enabled
- Workload Profile: Custom
- Sub-NUMA Clustering: Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on r120h2e Tue Jul 10 00:41:55 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name : Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
- 2 "physical id"s (chips)
- 32 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- cpu cores : 8
- siblings : 16
- physical 0: cores 0 1 2 3 4 5 6 7
- physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:

- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 32
- On-line CPU(s) list: 0-31
- Thread(s) per core: 2
- Core(s) per socket: 8
- Socket(s): 2
- NUMA node(s): 2

(Continued on next page)
**SPEC CPU2017 Floating Point Rate Result**

**NEC Corporation**

**Express5800/R120h-2E (Intel Xeon Silver 4108)**

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**CPU2017 License:** 9006  
**Test Sponsor:** NEC Corporation  
**Tested by:** NEC Corporation  
**Test Date:** Jul-2018  
**Hardware Availability:** Nov-2017  
**Software Availability:** Mar-2018

### Platform Notes (Continued)

- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
- **Stepping:** 4
- **CPU MHz:** 1800.000
- **BogoMIPS:** 3600.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 11264K
- **NUMA node0 CPU(s):** 0-7,16-23
- **NUMA node1 CPU(s):** 8-15,24-31
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx flc rdrand lahf_lm abm 3dnowprefetch epb cat_l3 cdp_l3 invpcid_single intel_pt spec_ctrl ibpb_support tpr_shadow vmni flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ertes invpced rtm cmqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cmqm_llc cmqm_occup_llc cmqm_mbx_total cmqm_mbx_local dtherm ida arat pln pts

From `numactl --hardware`

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

<table>
<thead>
<tr>
<th>node</th>
<th>cpus</th>
<th>size</th>
<th>free</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>0-1</td>
<td>97964 MB</td>
<td>95345 MB</td>
</tr>
<tr>
<td>1</td>
<td>8-15</td>
<td>98303 MB</td>
<td>95964 MB</td>
</tr>
</tbody>
</table>

From `/proc/meminfo`

```
MemTotal: 197749572 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```
Platform Notes (Continued)

From /etc/*release* /etc/*version*

```
  os-release:
    NAME="Red Hat Enterprise Linux Server"
    VERSION="7.4 (Maipo)"
    ID="rhel"
    ID_LIKE="fedora"
    VARIANT="Server"
    VARIANT_ID="server"
    VERSION_ID="7.4"
    PRETTY_NAME="Red Hat Enterprise Linux Server 7.4 (Maipo)"
  redhat-release: Red Hat Enterprise Linux Server release 7.4 (Maipo)
  system-release: Red Hat Enterprise Linux Server release 7.4 (Maipo)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:7.4:ga:server
```

```
uname -a:
    Linux r120h2e 3.10.0-693.21.1.el7.x86_64 #1 SMP Fri Feb 23 18:54:16 UTC 2018 x86_64
    x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- CVE-2017-5754 (Meltdown): Mitigation: PTI
- CVE-2017-5753 (Spectre variant 1): Mitigation: Load fences
- CVE-2017-5715 (Spectre variant 2): Mitigation: IBRS (kernel)

```
run-level 3 Jul 10 00:36
```

SPEC is set to: /home/cpu2017

```
Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda3      ext4  542G  314G  201G  62% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- BIOS NEC U31 02/14/2018
- Memory:
  - 4x UNKNOWN NOT AVAILABLE
  - 12x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

```
CC  519.lbm_r(base) 538.imagick_r(base, peak) 544.nab_r(base, peak)
```
### NEC Corporation

**Express5800/R120h-2E (Intel Xeon Silver 4108)**

<table>
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**CPU2017 License:** 9006  
**Test Sponsor:** NEC Corporation  
**Test Date:** Jul-2018  
**Hardware Availability:** Nov-2017  
**Tested by:** NEC Corporation  
**Software Availability:** Mar-2018

### Compiler Version Notes (Continued)

```plaintext
icc (ICC) 18.0.2 20180210
Copyright (C) 1985–2018 Intel Corporation. All rights reserved.

CC  519.lbm_r(peak)

icc (ICC) 18.0.2 20180210
Copyright (C) 1985–2018 Intel Corporation. All rights reserved.

CXXC 508.namd_r(base) 510.parest_r(base, peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985–2018 Intel Corporation. All rights reserved.

CXXC 508.namd_r(peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985–2018 Intel Corporation. All rights reserved.

CC  511.povray_r(base) 526.blender_r(base, peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985–2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985–2018 Intel Corporation. All rights reserved.

CC  511.povray_r(peak)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985–2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985–2018 Intel Corporation. All rights reserved.

FC  507.cactuBSSN_r(base, peak)

icpc (ICC) 18.0.2 20180210

(Continued on next page)
NEC Corporation

Express5800/R120h-2E (Intel Xeon Silver 4108)

SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

NEC Corporation

NEC Corporation

SPECrates2017_fp_base = 81.7
SPECrates2017_fp_peak = 83.9

CPU2017 License: 9006
Test Sponsor: NEC Corporation
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Test Date: Jul-2018
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Compiler Version Notes (Continued)

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------

==============================================================================

FC 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base)

==============================================================================

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------

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FC 554.roms_r(peak)

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------------------------------------------------------------------------------

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Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

(Continued on next page)
Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -ipo -03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:
-xCORE-AVX2 -ipo -03 -no-prec-div -qopt-prefetch -ffinite-math-only
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**NEC Corporation**  
**Express5800/R120h-2E (Intel Xeon Silver 4108)**  

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---

**Base Optimization Flags (Continued)**

Fortran benchmarks (continued):
- `-qopt-mem-layout-trans=3`  
- `-auto -nostandard-realloc-lhs`

Benchmarks using both Fortran and C:
- `-xCORE-AVX2`  
- `-ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only`  
- `-qopt-mem-layout-trans=3`  
- `-auto -nostandard-realloc-lhs`

Benchmarks using both C and C++:
- `-xCORE-AVX2`  
- `-ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only`  
- `-qopt-mem-layout-trans=3`

Benchmarks using Fortran, C, and C++:
- `-xCORE-AVX2`  
- `-ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only`  
- `-qopt-mem-layout-trans=3`  
- `-auto -nostandard-realloc-lhs`

---

**Peak Compiler Invocation**

**C benchmarks:**
- `icc -m64 -std=c11`

**C++ benchmarks:**
- `icpc -m64`

**Fortran benchmarks:**
- `ifort -m64`

Benchmarks using both Fortran and C:
- `ifort -m64 icc -m64 -std=c11`

Benchmarks using both C and C++:
- `icpc -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
- `icpc -m64 icc -m64 -std=c11 ifort -m64`

---

**Peak Portability Flags**

Same as Base Portability Flags
SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

NEC Corporation

Express5800/R120h-2E (Intel Xeon Silver 4108)

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CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Jul-2018
Hardware Availability: Nov-2017
Software Availability: Mar-2018

Peak Optimization Flags

C benchmarks:

519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

Fortran benchmarks:

503.bwaves_r: basepeak = yes

549.fotonik3d_r: basepeak = yes

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

526.blender_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:

(Continued on next page)
NEC Corporation

Express5800/R120h-2E (Intel Xeon Silver 4108)

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CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Jul-2018
Hardware Availability: Nov-2017
Software Availability: Mar-2018

Peak Optimization Flags (Continued)

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-R120h-RevB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-R120h-RevB.xml

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Tested with SPEC CPU2017 v1.0.5 on 2018-07-09 11:41:54-0400.
Originally published on 2018-08-07.