# SPEC® CPU2017 Integer Rate Result

**NEC Corporation**

Express5800/D120h (Intel Xeon Silver 4110)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9006</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>NEC Corporation</td>
</tr>
<tr>
<td>Tested by:</td>
<td>NEC Corporation</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Jul-2018</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Jan-2018</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2018</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>SPECrate2017_int_base = 37.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_int_peak = 39.5</td>
</tr>
</tbody>
</table>

## Hardware

- **CPU Name:** Intel Xeon Silver 4110
- **Max MHz.:** 3000
- **Nominal:** 2100
- **Enabled:** 8 cores, 1 chip, 2 threads/core
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per chip
- **Other:** None
- **Memory:** 192 GB (6 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Storage:** 1 x 1 TB SATA, 7200 RPM
- **Other:** None

## Software

- **OS:** Red Hat Enterprise Linux Server release 7.4 (Maipo)
- **Kernel:** 3.10.0-693.21.1.el7.x86_64
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Firmware:** Version F21 02/22/2018 released Apr-2018
- **File System:** ext4
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator library V5.0.1

## Benchmarks

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate2017_int_base</th>
<th>SPECrate2017_int_peak</th>
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<tbody>
<tr>
<td>500.perlbench_r</td>
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Copyright 2017-2018 Standard Performance Evaluation Corporation
Results Table

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<tr>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets;
jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
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Express5800/D120h (Intel Xeon Silver 4110)

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**CPU2017 License:** 9006  
**Test Sponsor:** NEC Corporation  
**Hardware Availability:** Jan-2018  
**Software Availability:** Mar-2018

**Test Date:** Jul-2018  
**Tested by:** NEC Corporation

---

### General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

---

### Platform Notes

**BIOS Settings:**
- ENERGY_PERF_BIAS_CFG mode: Performance
- LLC dead line alloc: Disable
- Patrol Scrub: Disable
- Sysinfo program /home/cpu2017/bin/sysinfo
- Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
- running on d120h Tue Jul 10 08:38:55 2018

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see [https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz
- 1 "physical id"s (chips)
- 16 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- cpu cores : 8
- siblings : 16
- physical 0: cores 0 1 2 3 4 5 6 7

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 16
- On-line CPU(s) list: 0-15
- Thread(s) per core: 2
- Core(s) per socket: 8
- Socket(s): 1
- NUMA node(s): 1
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz
- Stepping: 4
- CPU MHz: 2258.894

(Continued on next page)
## NEC Corporation

**Express5800/D120h (Intel Xeon Silver 4110)**

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### Platform Notes (Continued)

- **CPU max MHz:** 3000.0000  
- **CPU min MHz:** 800.0000  
- **BogoMIPS:** 4200.00  
- **Virtualization:** VT-x  
- **L1d cache:** 32K  
- **L1i cache:** 32K  
- **L2 cache:** 1024K  
- **L3 cache:** 11264K  
- **NUMA node0 CPU(s):** 0-15  
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid mxrs mgx smm mmxextf sse2 sse4_1 f16c tsc_adjust bmi1 hle avx2 smep bmi2  invpcid rtm cqm mpx mmxplus msr慰问 aid pdel vmpsat vsxmi f16c pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid mxrs mgx smm mmxextf sse2 sse4_1 f16c tsc_adjust bmi1 hle avx2 smep bmi2  invpcid rtm cqm mpx mmxplus msr慰问 aid pdel vmpsat vsxmi

From `numactl --hardware`  
**WARNING:** a numactl 'node' might or might not correspond to a physical chip.  
**available:** 1 nodes (0)  
**node 0 cpus:** 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15  
**node 0 size:** 195236 MB  
**node 0 free:** 190152 MB  
**node distances:**  
| node | 0 | 10 |

From `/proc/meminfo`  
**MemTotal:** 196476840 kB  
**HugePages_Total:** 0  
**Hugepagesize:** 2048 kB

From `/etc/*release`  
**os-release:**  
**NAME="Red Hat Enterprise Linux Server"**  
**VERSION="7.4 (Maipo)"**  
**ID="rhel"**  
**ID_LIKE="fedora"**  
**VARIANT="Server"**  
**VARIANT_ID="server"**

(Continued on next page)
### Platform Notes (Continued)

- VERSION_ID="7.4"
- PRETTY_NAME="Red Hat Enterprise Linux Server 7.4 (Maipo)"
- redhat-release: Red Hat Enterprise Linux Server release 7.4 (Maipo)
- system-release: Red Hat Enterprise Linux Server release 7.4 (Maipo)

```bash
uname -a:
Linux d120h 3.10.0-693.21.1.el7.x86_64 #1 SMP Fri Feb 23 18:54:16 UTC 2018 x86_64
x86_64 x86_64 GNU/Linux
```

run-level 3 Jul 10 08:33

SPEC is set to: /home/cpu2017

Filesystem    Type  Size  Used Avail Use% Mounted on
/dev/sda3      ext4  909G  401G  462G  47% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- BIOS GIGABYTE F21 02/22/2018
- Memory:
  10x NO DIMM NO DIMM
  6x Samsung M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

### Compiler Version Notes

```
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
  525.x264_r(base, peak) 557.xz_r(base, peak)
```

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

```
CC  500.perlbench_r(peak) 502.gcc_r(peak)
```

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

```
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
```
NEC Corporation
Express5800/D120h (Intel Xeon Silver 4110)

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Compiler Version Notes (Continued)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
541.leela_r(peak)
==============================================================================

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
FC 548.exchange2_r(base, peak)
==============================================================================

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64

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Base Portability Flags (Continued)

557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
- Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div 
- qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
- Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div 
- qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
- Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div 
- qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte 
- L/usr/local/je5.0.1-64/lib -ljemalloc

Base Other Flags

C benchmarks:
- m64 -std=c11

C++ benchmarks:
- m64

Fortran benchmarks:
- m64

Peak Compiler Invocation

C benchmarks:
- icc

C++ benchmarks:
- icpc

Fortran benchmarks:
- ifort
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<td><code>-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -fno-strict-overflow -L/usr/local/je5.0.1-64/lib -ljemalloc</code></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td><code>-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc</code></td>
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<tr>
<td>520.omnetpp_r</td>
<td><code>-basepeak = yes</code></td>
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<tr>
<td>523.xalancbmk_r</td>
<td><code>-L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-32/lib -ljemalloc</code></td>
</tr>
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### C++ benchmarks:

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<tr>
<td>525.x264_r</td>
<td><code>-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -fno-alias -L/usr/local/je5.0.1-64/lib -ljemalloc</code></td>
</tr>
<tr>
<td>557.xz_r</td>
<td><code>Same as 505.mcf_r</code></td>
</tr>
</tbody>
</table>

(Continued on next page)
SPEC CPU2017 Integer Rate Result

NEC Corporation

Express5800/D120h (Intel Xeon Silver 4110)

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>SPECrate2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>37.4</td>
<td>39.5</td>
</tr>
</tbody>
</table>

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Jul-2018
Hardware Availability: Jan-2018
Software Availability: Mar-2018

Peak Optimization Flags (Continued)

531.deepsjeng_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo 
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 
-L/usr/local/je5.0.1-64/lib -ljemalloc

541.leela_r: Same as 531.deepsjeng_r

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div 
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte 
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Other Flags

C benchmarks (except as noted below):
-m64 -std=c11

502.gcc_r: -m32 -std=c11

C++ benchmarks (except as noted below):
-m64

523.xalancbmk_r: -m32

Fortran benchmarks:
-m64

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-D120h-RevA.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-D120h-RevA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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