Supermicro
SuperStorage 5049P-E1CR45H (X11SPL-F, Intel Xeon Silver 4114)

SPECratenint_base = 46.7
SPECratenint_peak = 49.7

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro
Hardware Availability: Jul-2017
Software Availability: Mar-2018
Test Date: Oct-2018

Hardware
CPU Name: Intel Xeon Silver 4114
Max MHz.: 3000
Nominal: 2200
Enabled: 10 cores, 1 chip, 2 threads/core
Orderable: 1 chip
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 13.75 MB I+D on chip per chip
Other: None
Memory: 192 GB (6 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)
Storage: 1 x 200 GB SATA III SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 12 SP3 (x86_64)
Kernel 4.4.114-94.11-default
Compiler: C/C++: Version 18.0.2.199 of Intel C/C++
Compiler for Linux:
Fortran: Version 18.0.2.199 of Intel Fortran
Compiler for Linux:
Parallel: No
Firmware: Supermicro BIOS version 2.1 released Jun-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator library V5.0.1
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>548.exchange2_r</td>
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<td>33.5</td>
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<td>33.6</td>
</tr>
</tbody>
</table>

### Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
Supermicro
SuperStorage 5049P-E1CR45H (X11SPL-F, Intel Xeon Silver 4114)

SPECrate\textsubscript{2017\_int\_peak} = 49.7
SPECrate\textsubscript{2017\_int\_base} = 46.7

\begin{tabular}{|c|c|}
\hline
CPU2017 License: & 001176 \hline
Test Sponsor: & Supermicro \hline
Tested by: & Supermicro \hline
Test Date: & Oct-2018 \hline
Hardware Availability: & Jul-2017 \hline
Software Availability: & Mar-2018 \hline
\end{tabular}

General Notes (Continued)

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
LLC prefetch = Enable
Power Technology = Custom
Power Performance Tuning = BIOS Controls EPB
ENERGY\_PERF\_BIAS\_CFG mode = Maximum Performance
Hardware P-state = Out of Band Mode
XPT Prefetch = Enable
Stale AtoS = Enable
LLC dead line alloc = Disable
SDDC Plus One = Disable
ADDC Sparing = Disable
Patrol Scrub = Disable
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-52ma Mon Oct 8 15:30:15 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
\texttt{model name : Intel(R) Xeon(R) Silver 4114 CPU @ 2.20GHz}
\texttt{1 "physical id"\_s (chips)}
\texttt{20 "processors"}
\texttt{cores, siblings (Caution: counting these is hw and system dependent. The following exceptions from /proc/cpuinfo might not be reliable. Use with caution.)}
\texttt{cpu cores : 10}
\texttt{siblings : 20}
\texttt{physical 0: cores 0 1 2 3 4 8 9 10 11 12}

From lscpu:
\texttt{Architecture: \hspace{1cm} x86\_64}
\texttt{CPU op-mode(s): \hspace{1cm} 32\_bit, 64\_bit}
\texttt{Byte Order: \hspace{1cm} Little Endian}
\texttt{CPU(s): \hspace{1cm} 20}
\texttt{On\_line CPU(s) list: \hspace{1cm} 0\_19}
\texttt{Thread(s) per core: \hspace{1cm} 2}
\texttt{Core(s) per socket: \hspace{1cm} 10}
\texttt{Socket(s): \hspace{1cm} 1}
\texttt{NUMA node(s): \hspace{1cm} 1}

(Continued on next page)
SPEC CPU2017 Integer Rate Result

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Supermicro
SuperStorage 5049P-E1CR45H (X11SPL-F, Intel Xeon Silver 4114)

SPECrate2017_int_base = 46.7
SPECrate2017_int_peak = 49.7

Platform Notes (Continued)

Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4114 CPU @ 2.20GHz
Stepping: 4
CPU MHz: 2200.010
BogoMIPS: 4400.02
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-19
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good ntop nonstop_tsc
aarch64 aam hlt sysinv mmci cmov fell nonflushable disable gnu_callrax

From /proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 1 nodes (0)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
  node 0 size: 192078 MB
  node 0 free: 191379 MB
  node distances:
    node 0
    0: 10

From /proc/meminfo
  MemTotal: 196687880 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 3

(Continued on next page)
SPEC CPU2017 Integer Rate Result

Supermicro
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CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

Platform Notes (Continued)

# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

os-release:
  NAME="SLES"
  VERSION="12-SP3"
  VERSION_ID="12.3"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP3"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp3"

uname -a:
  Linux linux-52ma 4.4.114-94.11-default #1 SMP Thu Feb 1 19:28:26 UTC 2018 (4309ff9)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Mitigation: PTI
CVE-2017-5753 (Spectre variant 1): Mitigation: Barriers
CVE-2017-5715 (Spectre variant 2): Mitigation: IBRS+IBPB

run-level 3 Oct 8 15:25

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used  Avail  Use%  Mounted on
  /dev/sda4   xfs   145G  48G  97G  33%  /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS American Megatrends Inc. 2.1 06/15/2018
Memory:
  2x NO DIMM NO DIMM
  6x Samsung M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC   500.perlbench_r(base)  502.gcc_r(base)  505.mcf_r(base)  525.x264_r(base)
  557.xz_r(base)
==============================================================================
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
## SPEC CPU2017 Integer Rate Result

**Supermicro**  
SuperStorage 5049P-E1CR45H (X11SPL-F, Intel Xeon Silver 4114)

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**CPU2017 License:** 001176  
**Test Sponsor:** Supermicro  
**Tested by:** Supermicro  
**Test Date:** Oct-2018  
**Hardware Availability:** Jul-2017  
**Software Availability:** Mar-2018

### Compiler Version Notes (Continued)

```plaintext
---

CC  500.perlbench_r(peak) 502.gcc_r(peak) 505.mcf_r(peak) 525.x264_r(peak)  
     557.xz_r(peak)
---

icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)  
     541.leela_r(base)
---

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)  
     541.leela_r(peak)
---

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

FC  548.exchange2_r(base)
---

ifort (IFORT) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

FC  548.exchange2_r(peak)
---

ifort (IFORT) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---
```

### Base Compiler Invocation

C benchmarks:  
```bash
icc -m64 -std=c11
```

(Continued on next page)
## SPEC CPU2017 Integer Rate Result

**Supermicro**  
SuperStorage 5049P-E1CR45H (X11SPL-F, Intel Xeon Silver 4114)

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**CPU2017 License:** 001176  
**Test Sponsor:** Supermicro  
**Tested by:** Supermicro

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</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2018</td>
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</table>

### Base Compiler Invocation (Continued)

- **C++ benchmarks:**  
  icpc -m64

- **Fortran benchmarks:**  
  ifort -m64

### Base Portability Flags

- 500.perlbench_r: `--DSPEC_LP64 --DSPEC_LINUX_X64`
- 502.gcc_r: `--DSPEC_LP64`
- 505.mcf_r: `--DSPEC_LP64`
- 520.omnetpp_r: `--DSPEC_LP64`
- 523.xalancbmk_r: `--DSPEC_LP64 --DSPEC_LINUX`
- 525.x264_r: `--DSPEC_LP64`
- 531.deepsjeng_r: `--DSPEC_LP64`
- 541.leela_r: `--DSPEC_LP64`
- 548.exchange2_r: `--DSPEC_LP64`
- 557.xz_r: `--DSPEC_LP64`

### Base Optimization Flags

- **C benchmarks:**  
  -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

- **C++ benchmarks:**  
  -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

- **Fortran benchmarks:**  
  -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=3 -nostandard-realloc-lhs  
  -L/usr/local/je5.0.1-64/lib -ljemalloc

### Peak Compiler Invocation

- **C benchmarks (except as noted below):**  
  icc -m64 -std=c11

(Continued on next page)
Peak Compiler Invocation (Continued)

C++ benchmarks (except as noted below):

icpc -m64

523.xalancbmk_r icpc -m32 -L/home/prasadj/specdev/IC18u2_Internal/lin_18_0_20180210/compiler/lib/ia32_lin

Fortran benchmarks:

ifort -m64

Peak Portability Flags

C benchmarks:

500.perlbench_r: -D SPEC_LP64 -D SPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -D SPEC_LP64
520.omnetpp_r: -D SPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -D SPEC_LINUX
525.x264_r: -D SPEC_LP64
531.deepsjeng_r: -D SPEC_LP64
541.leela_r: -D SPEC_LP64
548.exchange2_r: -D SPEC_LP64
557.xz_r: -D SPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib
-ljemalloc

502.gcc_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-fno-alias -L/usr/local/je5.0.1-64/lib -ljemalloc

(Continued on next page)
# SPEC CPU2017 Integer Rate Result

## Supermicro

SuperStorage 5049P-E1CR45H (X11SPL-F, Intel Xeon Silver 4114)

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| Test Sponsor:          | Supermicro            |
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| Test Date:             | Oct-2018              |
| Hardware Availability: | Jul-2017              |
| Software Availability: | Mar-2018              |

### Peak Optimization Flags (Continued)

557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: basepeak = yes

541.leela_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2018-10-08 03:30:14-0400.
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