Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6150 2.70 GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default</td>
<td>CPU Name: Intel Xeon Gold 6150</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux</td>
<td>Max MHz.: 3700</td>
</tr>
<tr>
<td>Firmware: Version 3.2.3c released Mar-2018</td>
<td>Nominal: 2700</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Enabled: 72 cores, 4 chips</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Orderable: 2,4 Chips</td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Other: jemalloc: jemalloc memory allocator library V5.0.1;</td>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

SPECspeed2017_int_base = 8.88
SPECspeed2017_int_peak = 9.13
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6150 2.70 GHz)

SPECspeed2017_int_base = 8.88
SPECspeed2017_int_peak = 9.13

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>72</td>
<td>288</td>
<td>6.17</td>
<td>287</td>
<td>6.19</td>
<td>286</td>
<td>6.20</td>
<td>72</td>
<td>240</td>
<td>7.39</td>
<td>240</td>
<td>7.38</td>
<td>240</td>
<td>7.39</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>72</td>
<td>439</td>
<td>10.7</td>
<td>431</td>
<td>10.9</td>
<td>430</td>
<td>10.9</td>
<td>72</td>
<td>428</td>
<td>11.0</td>
<td>427</td>
<td>11.1</td>
<td>436</td>
<td>10.8</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>72</td>
<td>254</td>
<td>6.43</td>
<td>274</td>
<td>6.96</td>
<td>259</td>
<td>6.30</td>
<td>72</td>
<td>249</td>
<td>6.54</td>
<td>256</td>
<td>6.37</td>
<td>267</td>
<td>6.10</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>72</td>
<td>149</td>
<td>9.50</td>
<td>150</td>
<td>9.44</td>
<td>148</td>
<td>9.56</td>
<td>72</td>
<td>140</td>
<td>10.1</td>
<td>141</td>
<td>10.0</td>
<td>140</td>
<td>10.1</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>72</td>
<td>150</td>
<td>11.7</td>
<td>150</td>
<td>11.8</td>
<td>150</td>
<td>11.7</td>
<td>72</td>
<td>150</td>
<td>11.8</td>
<td>150</td>
<td>11.8</td>
<td>150</td>
<td>11.8</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>72</td>
<td>285</td>
<td>5.02</td>
<td>285</td>
<td>5.03</td>
<td>285</td>
<td>5.03</td>
<td>72</td>
<td>286</td>
<td>5.01</td>
<td>287</td>
<td>5.00</td>
<td>286</td>
<td>5.00</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>72</td>
<td>393</td>
<td>4.34</td>
<td>393</td>
<td>4.34</td>
<td>392</td>
<td>4.35</td>
<td>72</td>
<td>391</td>
<td>4.36</td>
<td>391</td>
<td>4.36</td>
<td>391</td>
<td>4.36</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>72</td>
<td>219</td>
<td>13.4</td>
<td>219</td>
<td>13.4</td>
<td>220</td>
<td>13.4</td>
<td>72</td>
<td>220</td>
<td>13.4</td>
<td>219</td>
<td>13.4</td>
<td>220</td>
<td>13.4</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>72</td>
<td>258</td>
<td>24.0</td>
<td>261</td>
<td>23.7</td>
<td>262</td>
<td>23.6</td>
<td>72</td>
<td>258</td>
<td>24.0</td>
<td>260</td>
<td>23.7</td>
<td>261</td>
<td>23.7</td>
</tr>
</tbody>
</table>

SPECspeed2017_int_base = 8.88
SPECspeed2017_int_peak = 9.13

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64:/opt/cpu2017/je5.0.1-32:/opt/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc: configured and built at default for
32bit (i686) and 64bit (x86_64) targets;
jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;
jemalloc: sources available from jemalloc.net or

(Continued on next page)
### General Notes (Continued)


### Platform Notes

**BIOS Settings:**
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- Patrol Scrub set to Disabled

**Sysinfo program /opt/cpu2017/bin/sysinfo**
```
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-vb5q Sun Oct 21 21:30:32 2018
```

**SUT (System Under Test) info as seen by some common utilities.**

For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

**From /proc/cpuinfo**
```
model name : Intel(R) Xeon(R) Gold 6150 CPU @ 2.70GHz
  4 "physical id"s (chips)
  72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 18
  siblings : 18
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 2: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 3: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
```

**From lscpu:**
```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                72
On-line CPU(s) list:   0-71
Thread(s) per core:    1
Core(s) per socket:    18
Socket(s):             4
NUMA node(s):          4
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Gold 6150 CPU @ 2.70GHz
Stepping:              4
```

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6150 2.70 GHz)

SPECspeed2017_int_base = 8.88
SPECspeed2017_int_peak = 9.13

Platform Notes (Continued)

CPU MHz: 2481.631
CPU max MHz: 3700.000
CPU min MHz: 1200.000
BogoMIPS: 5399.98
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-17
NUMA node1 CPU(s): 18-35
NUMA node2 CPU(s): 36-53
NUMA node3 CPU(s): 54-71

Flags: fpu vme mpx cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx mdtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abml rm cx8 apic cpuid cmov

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
ode 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 385463 MB
node 0 free: 383759 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 387057 MB
node 1 free: 383512 MB
node 2 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
node 2 size: 387057 MB
node 2 free: 385073 MB
node 3 cpus: 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 3 size: 387054 MB
node 3 free: 384866 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6150 2.70 GHz)  

**SPEC CPU2017 Integer Speed Result**

**Cisco Systems**

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

<table>
<thead>
<tr>
<th>Spec</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_base</td>
<td>8.88</td>
</tr>
<tr>
<td>SPECspeed2017_int_peak</td>
<td>9.13</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

3: 21 21 21 10

From `/proc/meminfo`
- MemTotal: 1583751252 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release* /etc/*version*`
- SuSE-release:
  - SUSE Linux Enterprise Server 12 (x86_64)
  - VERSION = 12
  - PATCHLEVEL = 2
  - # This file is deprecated and will be removed in a future service pack or release.
  - # Please check /etc/os-release for details about this release.
- os-release:
  - NAME="SLES"
  - VERSION="12-SP2"
  - VERSION_ID="12.2"
  - PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  - ID="sles"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:12:sp2"

`uname -a`:
- Linux linux-vb5q 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
  - x86_64 x86_64 x86_64 GNU/Linux

`run-level` 3 Oct 21 19:36

`SPEC is set to: /opt/cpu2017`

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sdal</td>
<td>xfs</td>
<td>280G</td>
<td>84G</td>
<td>197G</td>
<td>30%</td>
<td>/</td>
</tr>
</tbody>
</table>

Additional information from `dmidecode` follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**BIOS** Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018

**Memory:**
- 48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6150 2.70 GHz)

SPEC CPU2017 Integer Speed Result
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Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6150 2.70 GHz)

SPECspeed2017_int_base = 8.88
SPECspeed2017_int_peak = 9.13

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2018
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Mar-2018

Compiler Version Notes
==============================================================================
CC  600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base, peak) 657.xz_s(base)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
CC  600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base) 641.leela_s(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
CXXC 620.omnetpp_s(peak) 623.xalancbmk_s(peak) 631.deepsjeng_s(peak) 641.leela_s(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
FC  648.exchange2_s(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
Base Compiler Invocation
C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
icpc -m64

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6150
2.70 GHz)

SPECspeed2017_int_base = 8.88
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Oct-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64

(Continued on next page)
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SPECspeed2017_int_base = 8.88  
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CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Oct-2018  
Hardware Availability: Aug-2017  
Software Availability: Mar-2018

Peak Compiler Invocation (Continued)
623.xalancbmk_s: icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
Fortran benchmarks:
ifort -m64

Peak Portability Flags
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
602.gcc_s: -DSPEC_LP64  
605.mcf_s: -DSPEC_LP64  
620.omnetpp_s: -DSPEC_LP64  
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
625.x264_s: -DSPEC_LP64  
631.deepsjeng_s: -DSPEC_LP64  
641.leea_s: -DSPEC_LP64  
648.exchange2_s: -DSPEC_LP64  
657.xz_s: -DSPEC_LP64

Peak Optimization Flags
C benchmarks:
600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -fno-strict-overflow  
-L/usr/local/je5.0.1-64/lib -ljemalloc  
602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc  
605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc  
625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

(Continued on next page)
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2018
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Peak Optimization Flags (Continued)

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

623.xalancbmk_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-32/lib -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2018-10-21 21:30:32-0400.