## SPEC® CPU2017 Floating Point Speed Result

### Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 5122 3.60 GHz)

<table>
<thead>
<tr>
<th>Threads</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
</tr>
<tr>
<td>619.ibm_s</td>
</tr>
<tr>
<td>621.wrf_s</td>
</tr>
<tr>
<td>627.cam4_s</td>
</tr>
<tr>
<td>628.pop2_s</td>
</tr>
<tr>
<td>638.imagick_s</td>
</tr>
<tr>
<td>644.nab_s</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
</tr>
<tr>
<td>654.roms_s</td>
</tr>
</tbody>
</table>

| SPECspeed2017_fp_base | 84.3 |
| SPECspeed2017_fp_peak | 84.9 |

### CPU2017 License: 9019
Test Date: Nov-2018
Test Sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Mar-2018

### Hardware
CPU Name: Intel Xeon Gold 5122
Max MHz.: 3700
Nominal: 3600
Enabled: 16 cores, 4 chips
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 16.5 MB I+D on chip per chip
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 400 GB SSD SAS
Other: None

### Software
OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 3.2.3c released Mar-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
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### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Base</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
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<td>122</td>
<td>482</td>
<td>482</td>
<td>123</td>
<td>480</td>
<td>122</td>
<td>484</td>
<td>16</td>
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<td>485</td>
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<td>607.cactubssn_s</td>
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<td>206</td>
<td>81.1</td>
<td>205</td>
<td>81.5</td>
<td>206</td>
<td>80.7</td>
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<td>81.2</td>
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<td>85.8</td>
<td>61.1</td>
<td>85.3</td>
<td>61.4</td>
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<td>86.7</td>
<td>60.4</td>
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<td>621.wrf_s</td>
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<td>233</td>
<td>56.8</td>
<td>231</td>
<td>57.2</td>
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<td>56.4</td>
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<td>248</td>
<td>56.7</td>
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<td>627.cam4_s</td>
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<td>171</td>
<td>52.0</td>
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<td>51.8</td>
<td>170</td>
<td>52.0</td>
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<td>171</td>
<td>51.7</td>
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<td>248</td>
<td>47.8</td>
<td>253</td>
<td>16</td>
<td>253</td>
<td>48.0</td>
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<tr>
<td>638.imagick_s</td>
<td>16</td>
<td>237</td>
<td>60.8</td>
<td>237</td>
<td>60.7</td>
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<td>60.5</td>
<td>242</td>
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<td>60.3</td>
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<td>16</td>
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<td>163</td>
<td>16</td>
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<td>107</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
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<td>86.5</td>
<td>105</td>
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<td>16</td>
<td>105</td>
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<tr>
<td>654.roms_s</td>
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<td>96.2</td>
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<td>93.1</td>
<td>166</td>
<td>94.9</td>
<td>159</td>
<td>16</td>
<td>159</td>
<td>98.8</td>
</tr>
</tbody>
</table>

**SPECspeed2017_fp_base =** 84.3  
**SPECspeed2017_fp_peak =** 84.9

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
- `KMP_AFFINITY = "granularity=fine,compact"
- `LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
- `OMP_STACKSIZE = "192M"

Bins compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:
```
sync; echo 3>/proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-xy4f Tue Nov  6 22:57:34 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
4 "physical id"s (chips)
16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 4
physical 0: cores 1 2 5 11
physical 1: cores 1 10 11 12
physical 2: cores 1 5 9 13
physical 3: cores 1 2 5 11

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 4
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
Stepping: 4
CPU MHz: 2641.656
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 7199.96
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K

(Continued on next page)
### Cisco Systems

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| Test Date                | Nov-2018      |
| Hardware Availability    | Aug-2017      |
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#### Platform Notes (Continued)

| L3 cache                | 16896K        |
| NUMA node0 CPU(s)       | 0-3           |
| NUMA node1 CPU(s)       | 4-7           |
| NUMA node2 CPU(s)       | 8-11          |
| NUMA node3 CPU(s)       | 12-15         |

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good ncpu xtopology nonstop_tsc aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xSAVE ax64 rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts dtherm hwp hwp_act_window hwp_epp hwp_kmg req intel_pt rsb_cxsw spec_ctrl stibp retpoline kaiser tpr_shadow vmx flexpriority ept vpid fsgsbase tsc_adjust bni hle avx2 smep bmi2 3ms invpcid single rtm cmq mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512vdavx512bw avx512vl xsaveopt xsavec xgetbv1 cmq_llc cmq occupancy

/proc/cpuinfo cache data
- cache size : 16896 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
- available: 4 nodes (0-3)
  - node 0 cpus: 0 1 2 3
  - node 0 size: 385624 MB
  - node 0 free: 382721 MB
  - node 1 cpus: 4 5 6 7
  - node 1 size: 387057 MB
  - node 1 free: 384620 MB
  - node 2 cpus: 8 9 10 11
  - node 2 size: 387057 MB
  - node 2 free: 386211 MB
  - node 3 cpus: 12 13 14 15
  - node 3 size: 387054 MB
  - node 3 free: 385249 MB
- node distances:
  - node 0 1 2 3
  - 0: 10 21 31 21
  - 1: 21 10 21 31
  - 2: 31 21 10 21
  - 3: 21 31 21 10

From /proc/meminfo
- MemTotal: 1583916388 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release*/etc/*version* (Continued on next page)
Cisco Systems
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SPECspeed2017_fp_base = 84.3
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Platform Notes (Continued)

SuSE-release:
   SUSE Linux Enterprise Server 12 (x86_64)
   VERSION = 12
   PATCHLEVEL = 2
   # This file is deprecated and will be removed in a future service pack or release.
   # Please check /etc/os-release for details about this release.

os-release:
   NAME="SLES"
   VERSION="12-SP2"
   VERSION_ID="12.2"
   PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
   ID="sles"
   ANSI_COLOR="0;32"
   CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-xy4f 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 1 23:07

SPEC is set to: /home/cpu2017

Filesystem     Type Size  Used Avail Use% Mounted on
/dev/sda1      xfs   224G 76G 148G 34% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
   Memory:
   48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
 CC 619.lbm_s(base) 638.imagick_s(base, peak) 644.nab_s(base, peak)
==============================================================================
 icc (ICC) 18.0.0 20170811
 Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
 CC 619.lbm_s(peak)

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 5122 3.60 GHz)

SPEC CPU2017 Floating Point Speed Result

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Cisco Systems

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Compiler Version Notes (Continued)

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
FC  607.cactuBSSN_s(base)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
FC  607.cactuBSSN_s(peak)

icpc (ICC) 18.0.0 20170811
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icc (ICC) 18.0.0 20170811
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ifort (IFORT) 18.0.0 20170811
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==============================================================================
FC  603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

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==============================================================================

CC  621.wrf_s(base) 627.cam4_s(base, peak) 628.pop2_s(base)

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Compiler Version Notes (Continued)
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==============================================================================
CC 621.wrf_s(peak) 628.pop2_s(peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
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---

### Base Optimization Flags

**C benchmarks:**  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

**Fortran benchmarks:**  
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp  
-nostandard-realloc-lhs -align array32byte

**Benchmarks using both Fortran and C:**  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs -align array32byte

**Benchmarks using Fortran, C, and C++:**  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs -align array32byte

---

### Peak Compiler Invocation

**C benchmarks:**  
icc -m64 -std=c11

**Fortran benchmarks:**  
ifort -m64

**Benchmarks using both Fortran and C:**  
ifort -m64 icc -m64 -std=c11

**Benchmarks using Fortran, C, and C++:**  
icpc -m64 icc -m64 -std=c11 ifort -m64

---

### Peak Portability Flags

Same as Base Portability Flags
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Software Availability: Mar-2018

Peak Optimization Flags

C benchmarks:
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:
-no-prec-gen(pass 1) -no-prec-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-no-prec-gen(pass 1) -no-prec-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch
-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml
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Tested with SPEC CPU2017 v1.0.2 on 2018-11-06 22:57:33-0500.
Originally published on 2018-11-27.