Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6128 3.40 GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default</td>
<td>CPU Name: Intel Xeon Gold 6128</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux</td>
<td>Max MHz.: 3700</td>
</tr>
<tr>
<td>Firmware: Version 3.2.3c released Mar-2018</td>
<td>Nominal: 3400</td>
</tr>
<tr>
<td>File System: xfs</td>
<td>Enabled: 24 cores, 4 chips</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Orderable: 2,4 Chips</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other: jemalloc memory allocator V5.0.1</td>
<td>L3: 19.25 MB I+D on chip per chip</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed2017_int_base</th>
<th>SPECspeed2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>6.24</td>
<td>7.31</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>9.03</td>
<td>9.31</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>10.9</td>
<td>11.0</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>5.45</td>
<td>5.63</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>9.48</td>
<td></td>
</tr>
<tr>
<td>625.x264_s</td>
<td>10.1</td>
<td>11.5</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>5.08</td>
<td>5.72</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>4.38</td>
<td>4.36</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>13.3</td>
<td>13.5</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>21.7</td>
<td>21.8</td>
</tr>
</tbody>
</table>

Test Sponsor: Cisco Systems
Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018
SPEC CPU2017 Integer Speed Result

Cisco Systems
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SPECspeed2017_int_base = 8.65
SPECspeed2017_int_peak = 8.90

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>24</td>
<td>290</td>
<td>6.12</td>
<td>282</td>
<td>6.29</td>
<td>284</td>
<td>6.24</td>
<td>24</td>
<td>243</td>
<td>7.31</td>
<td>240</td>
<td>7.39</td>
<td>244</td>
<td>7.28</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>24</td>
<td>441</td>
<td>9.03</td>
<td>438</td>
<td>9.10</td>
<td>443</td>
<td>8.98</td>
<td>24</td>
<td>427</td>
<td>9.33</td>
<td>432</td>
<td>9.21</td>
<td>428</td>
<td>9.31</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>24</td>
<td>432</td>
<td>10.9</td>
<td>436</td>
<td>10.8</td>
<td>434</td>
<td>10.9</td>
<td>24</td>
<td>429</td>
<td>11.0</td>
<td>430</td>
<td>11.0</td>
<td>434</td>
<td>10.9</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>24</td>
<td>299</td>
<td>5.45</td>
<td>284</td>
<td>5.75</td>
<td>302</td>
<td>5.41</td>
<td>24</td>
<td>289</td>
<td>5.46</td>
<td>290</td>
<td>5.63</td>
<td>282</td>
<td>5.78</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>24</td>
<td>150</td>
<td>9.47</td>
<td>150</td>
<td>9.48</td>
<td>148</td>
<td>9.54</td>
<td>24</td>
<td>141</td>
<td>10.1</td>
<td>141</td>
<td>10.0</td>
<td>140</td>
<td>10.1</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>24</td>
<td>221</td>
<td>13.3</td>
<td>221</td>
<td>13.3</td>
<td>221</td>
<td>13.3</td>
<td>24</td>
<td>217</td>
<td>13.6</td>
<td>217</td>
<td>13.5</td>
<td>217</td>
<td>13.5</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>24</td>
<td>282</td>
<td>5.08</td>
<td>282</td>
<td>5.08</td>
<td>282</td>
<td>5.09</td>
<td>24</td>
<td>286</td>
<td>5.01</td>
<td>285</td>
<td>5.02</td>
<td>286</td>
<td>5.02</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = ":/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64:/opt/cpu2017/je5.0.1-32:/opt/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
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Cisco Systems

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Tested by: Cisco Systems

CPU2017 License: 9019
Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

SPECspeed2017_int_base = 8.65
SPECspeed2017_int_peak = 8.90

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /opt/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b0910f0
running on linux-vb5q Sun Jan 3 09:04:13 2010

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
  4 "physical id"s (chips)
  24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 6
  siblings: 6
  physical 0: cores 0 6 9 10 11 13
  physical 1: cores 0 6 9 10 11 13
  physical 2: cores 0 6 9 10 11 13
  physical 3: cores 0 3 4 9 12 14

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 24
On-line CPU(s) list: 0-23
Thread(s) per core: 1
Core(s) per socket: 6
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
Stepping: 4
CPU MHz: 3172.699
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 6799.99
Virtualization: VT-x

(Continued on next page)
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CPU2017 License: 9019
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Test Date: Nov-2018

Platform Notes (Continued)

L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 19712K
NUMA node0 CPU(s): 0-5
NUMA node1 CPU(s): 6-11
NUMA node2 CPU(s): 12-17
NUMA node3 CPU(s): 18-23

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscl
lm constant tsart arch_perfmon pebs bts rep_good ntopology nonstop tsc
aperfmon perf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpcr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx fl64 rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow
vmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3hand invpcid
rtm cqm mpx avx512f avx512dq rdseed adx snapp clflushopt clwb avx512cd avx512bw
avx512vl xsaveopt xsaves xgetbv1 cqm_llc cqm_occupa llc

(proc/cpuinfo cache data

cache size : 19712 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5
node 0 size: 385463 MB
node 0 free: 385141 MB
node 1 cpus: 6 7 8 9 10 11
node 1 size: 387057 MB
node 1 free: 386770 MB
node 2 cpus: 12 13 14 15 16 17
node 2 size: 387057 MB
node 2 free: 386800 MB
node 3 cpus: 18 19 20 21 22 23
node 3 size: 387054 MB
node 3 free: 386866 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

From /proc/meminfo
MemTotal: 1583751444 kB
HugePages_Total: 0

(Continued on next page)
Cisco Systems
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SPECspeed2017_int_base = 8.65
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Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
    os-release:
        NAME="SLES"
        VERSION="12-SP2"
        VERSION_ID="12.2"
        PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
        ID="sles"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-vb5q 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
    x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 3 08:44

SPEC is set to: /opt/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 280G 77G 203G 28% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
Memory:
    48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base,
    peak) 657.xz_s(base)
==============================================================================
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6128 3.40 GHz)

SPEC CPU2017 Integer Speed Result
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<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Nov-2018</th>
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</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Mar-2018</td>
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</table>

**SPECspeed2017_int_base = 8.65**

**SPECspeed2017_int_peak = 8.90**

---

**Compiler Version Notes (Continued)**

---

```
CC 600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
```

```
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

```
CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
641.leela_s(base)
```

```
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

```
CXXC 620.omnetpp_s(peak) 623.xalancbmk_s(peak) 631.deepsjeng_s(peak)
641.leela_s(peak)
```

```
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

```
FC 648.exchange2_s(base, peak)
```

```
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

**Base Compiler Invocation**

C benchmarks:
\`
icc -m64 -std=c11
```

C++ benchmarks:
\`
icpc -m64
```

Fortran benchmarks:
\`
ifort -m64
```
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CPU2017 License: 9019
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Test Date: Nov-2018
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Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64

623.xalancbmk_s: icpc -m32 -L/home/prasad/specdev/IC18u2_Internal/lin_18_0_20180210/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64
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Cisco UCS B480 M5 (Intel Xeon Gold 6128 3.40 GHz)

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SPECspeed2017_int_peak = 8.90

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Tested by: Cisco Systems
Software Availability: Mar-2018

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leea_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -qopt-mem-layout-trans=3 -no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -fno-strict-overflow -L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -qopt-mem-layout-trans=3 -no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp

C++ benchmarks:
620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp

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Peak Optimization Flags (Continued)

620.omnetpp_s (continued):
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

623.xalancbmk_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-32/lib -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s
641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-L/usr/local/je5.0.1-64/lib -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2010-01-03 09:04:12-0500.
Originally published on 2018-11-27.