## SPEC® CPU2017 Integer Speed Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6142 2.60 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Nov-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
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<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
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</tbody>
</table>

### Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed2017_int_base</th>
<th>SPECspeed2017_int_peak</th>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>32</td>
<td>6.29</td>
<td>7.35</td>
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<tr>
<td>602.gcc_s</td>
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<td>9.29</td>
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<tr>
<td>605.mcf_s</td>
<td>32</td>
<td>6.01</td>
<td>6.02</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>32</td>
<td>9.52</td>
<td>10.2</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>32</td>
<td>13.0</td>
<td>13.0</td>
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<td>625.x264_s</td>
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<td>5.75</td>
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<tr>
<td>631.deepsjeng_s</td>
<td>32</td>
<td>4.53</td>
<td>4.50</td>
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<tr>
<td>641.leela_s</td>
<td>32</td>
<td>13.4</td>
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<tr>
<td>648.exchange2_s</td>
<td>32</td>
<td>21.8</td>
<td>21.9</td>
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<tr>
<td>657.xz_s</td>
<td>32</td>
<td>21.9</td>
<td>21.9</td>
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</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6142
- **Max MHz.:** 3700
- **Nominal:** 2600
- **Enabled:** 32 cores, 2 chips
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 400 GB SAS SSD
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.1 released Oct-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
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<th>Seconds</th>
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<td>220</td>
<td>13.4</td>
</tr>
</tbody>
</table>

SPECspeed2017_int_base = 8.96
SPECspeed2017_int_peak = 9.19

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
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Test Date: Nov-2018
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-klde Wed Dec  5 14:34:23 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6142 CPU @ 2.60GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6142 CPU @ 2.60GHz
Stepping: 4
CPU MHz: 3650.725
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 5187.80
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

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Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 22582K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
Flags: fpu vme de pse tsc msr pae mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmonperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epbi invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_kpp_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vmvi flexpriority vmpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 ermv invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
c1wb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc
cache size: 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385627 MB
node 0 free: 385208 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387054 MB
node 1 free: 386564 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 791226492 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SUSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"

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Platform Notes (Continued)

VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-klde 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 5 14:33

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda3      xfs   212G  114G   99G  54% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
Memory:
24x OxCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base, peak) 657.xz_s(base)
==============================================================================

icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================
CC  600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
==============================================================================

icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================
CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base) 641.leela_s(base)
(Continued on next page)
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Compiler Version Notes (Continued)

---

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

CXXC 620.omnetpp_s(peak) 623.xalancbmk_s(peak) 631.deepsjeng_s(peak) 641.leela_s(peak)
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

FC 648.exchange2_s(base, peak)
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
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Base Optimization Flags
C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

Peak Compiler Invocation
C benchmarks:
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64

623.xalancbmk_s: icpc -m32 -L/opt/intel/lib/ia32

Fortran benchmarks:
ifort -m64

Peak Portability Flags
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
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The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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