## SPEC® CPU2017 Integer Speed Result

### Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6128 3.40 GHz)

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

<table>
<thead>
<tr>
<th>Software</th>
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| OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default | CPU Name: Intel Xeon Gold 6128  
Max MHz.: 3700  
Nominal: 3400  
Enabled: 12 cores, 2 chips  
Orderable: 1,2 Chips  
Cache L1: 32 KB I + 32 KB D on chip per core  
L2: 1 MB I+D on chip per core  
L3: 19.25 MB I+D on chip per core |
| Compiler: C/C++: Version 19.0.1.144 of Intel C/C++  
Compiler for Linux: Fortran: Version 19.0.1.144 of Intel Fortran  
Compiler for Linux Compiler | Base Pointers: 64-bit  
Peak Pointers: 32/64-bit  
Other: jemalloc memory allocator V5.0.1 |
| Parallel: Yes  
Firmware: Version 4.0.1 released Oct-2018  
File System: xfs | System State: Run level 3 (multi-user) |

### SPECspeed2017_int_base = 8.57

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### Software Benchmark Results

<table>
<thead>
<tr>
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<th>Threads</th>
<th>SPECspeed2017_int_base</th>
<th>SPECspeed2017_int_peak</th>
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<tbody>
<tr>
<td>perlbench</td>
<td>12</td>
<td>7.50</td>
<td>10.2</td>
</tr>
<tr>
<td>gcc</td>
<td>12</td>
<td>9.19</td>
<td>13.0</td>
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<tr>
<td>mcf</td>
<td>12</td>
<td>9.39</td>
<td>12.9</td>
</tr>
<tr>
<td>omnetpp</td>
<td>12</td>
<td>9.47</td>
<td>12.4</td>
</tr>
<tr>
<td>xalancbmk</td>
<td>12</td>
<td>10.2</td>
<td>15.1</td>
</tr>
<tr>
<td>x264</td>
<td>12</td>
<td>13.0</td>
<td>15.3</td>
</tr>
<tr>
<td>deepsjeng</td>
<td>12</td>
<td>8.55</td>
<td>13.4</td>
</tr>
<tr>
<td>leela</td>
<td>12</td>
<td>4.52</td>
<td>13.4</td>
</tr>
<tr>
<td>exchange2</td>
<td>12</td>
<td>5.22</td>
<td>13.4</td>
</tr>
<tr>
<td>xz</td>
<td>12</td>
<td>5.69</td>
<td>5.65</td>
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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6128 3.40 GHz)

SPEC CPU2017 Integer Speed Result

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Cisco Systems

SPECspeed2017_int_base = 8.57
SPECspeed2017_int_peak = 8.80

Results Table

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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Seconds</th>
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<th>Ratio</th>
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<th>Ratio</th>
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<td>12</td>
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<td>6.26</td>
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<td>6.26</td>
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<td>6.28</td>
<td>12</td>
<td>237</td>
<td>7.50</td>
<td>238</td>
<td>7.45</td>
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<td>605.mcf_s</td>
<td>12</td>
<td>426</td>
<td>11.1</td>
<td>430</td>
<td>11.0</td>
<td>425</td>
<td>11.1</td>
<td>12</td>
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<td>11.1</td>
<td>425</td>
<td>11.1</td>
<td>433</td>
<td>10.9</td>
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<tr>
<td>620.omnetpp_s</td>
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<td>5.69</td>
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<td>5.59</td>
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<td>288</td>
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<td>150</td>
<td>9.43</td>
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<td>10.2</td>
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<tr>
<td>625.x264_s</td>
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<td>136</td>
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<td>136</td>
<td>13.0</td>
<td>136</td>
<td>13.0</td>
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<td>5.21</td>
<td>275</td>
<td>5.22</td>
<td>12</td>
<td>278</td>
<td>5.15</td>
<td>279</td>
<td>5.14</td>
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<td>5.15</td>
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<td>641.leela_s</td>
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<td>4.53</td>
<td>376</td>
<td>4.53</td>
<td>377</td>
<td>4.52</td>
<td>12</td>
<td>378</td>
<td>4.52</td>
<td>377</td>
<td>4.52</td>
<td>377</td>
<td>4.52</td>
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<tr>
<td>648.exchange2_s</td>
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<td>13.5</td>
<td>220</td>
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<td>12</td>
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<td>13.4</td>
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<td>13.4</td>
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<td>13.5</td>
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<tr>
<td>657.xz_s</td>
<td>12</td>
<td>411</td>
<td>15.0</td>
<td>410</td>
<td>15.1</td>
<td>408</td>
<td>15.2</td>
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<td>404</td>
<td>15.3</td>
<td>407</td>
<td>15.2</td>
<td>404</td>
<td>15.3</td>
</tr>
</tbody>
</table>

SPECspeed2017_int_base = 8.57
SPECspeed2017_int_peak = 8.80

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
## SPEC CPU2017 Integer Speed Result

### Cisco Systems

**Cisco UCS C240 M5 (Intel Xeon Gold 6128 3.40 GHz)**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_base</td>
<td>8.57</td>
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<tr>
<td>SPECspeed2017_int_peak</td>
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| License                | 9019      |
| Test Sponsor           | Cisco Systems |
| Tested by              | Cisco Systems |
| Test Date              | Nov-2018  |
| Hardware Availability  | Aug-2017  |
| Software Availability  | Oct-2018  |

### Platform Notes

**BIOS Settings:**
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- Patrol Scrub set to Disabled

**Sysinfo program**
/home/cpu2017/bin/sysinfo

Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bce091c0f
running on linux-dkz7 Thu Nov 29 02:10:05 2018

**SUT (System Under Test) info as seen by some common utilities.**

For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

**From /proc/cpuinfo**

```
model name : Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
  2 "physical id"s (chips)
  12 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 6
  siblings : 6
  physical 0: cores 0 6 9 10 11 13
  physical 1: cores 0 6 9 10 11 13
```

**From lscpu:**

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                12
On-line CPU(s) list:   0-11
Thread(s) per core:    1
Core(s) per socket:    6
Socket(s):             2
NUMA node(s):          2
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
Stepping:              4
CPU MHz:               1430.293
CPU max MHz:           3700.0000
CPU min MHz:           1200.0000
BogoMIPS:              6784.09
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
```

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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6128
3.40 GHz)

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**SPEC CPU2017 Integer Speed Result**

**SPECspeed2017_int_base = 8.57**

**SPECspeed2017_int_peak = 8.80**

Platform Notes (Continued)

- L2 cache: 1024K
- L3 cache: 19712K
- NUMA node0 CPU(s): 0-5
- NUMA node1 CPU(s): 6-11
- Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpica mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good ntopology nonstop_tsc aperfmpref eagerfpupi pclmulqdq dtc64s monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xptr pdcmd cpio dca ssse4_1 ssse4_2 x2apic movbe popcnt tsct_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp retopolhine kaiser tpr_shadow vmvpi flexpriority ept vpid fsgsbase tsc_adjust bni hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

From `numactl --hardware` WARNING: a numactl 'node' might or might not correspond to a physical chip.
- available: 2 nodes (0-1)
- node 0 cpus: 0 1 2 3 4 5
- node 0 size: 385626 MB
- node 0 free: 385189 MB
- node 1 cpus: 6 7 8 9 10 11
- node 1 size: 387054 MB
- node 1 free: 386605 MB
- node distances:
  - node 0 1
  - 0: 10 21
  - 1: 21 10

From `/proc/meminfo`
- MemTotal: 791225644 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release* /etc/*version*`
- SuSE-release:
  - SUSE Linux Enterprise Server 12 (x86_64)
  - VERSION = 12
  - PATCHLEVEL = 2
  - # This file is deprecated and will be removed in a future service pack or release.
  - # Please check /etc/os-release for details about this release.
- os-release:
  - NAME="SLES"
  - VERSION="12-SP2"

(Continued on next page)
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Platform Notes (Continued)

VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Nov 29 01:35

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda2      xfs   500G  118G  383G  24% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
Memory:
12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base, peak) 657.xz_s(base)
==============================================================================
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
CC  600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
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Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
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Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)

```
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

CXXC  620.omnetpp_s(peak)  623.xalancbmk_s(peak)  631.deepsjeng_s(peak)
   641.leela_s(peak)

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

FC  648.exchange2_s(base, peak)

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
```

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Base Portability Flags (Continued)

657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64
623.xalancbmk_s: icpc -m32 -L/opt/intel/lib/ia32

Fortran benchmarks:
ifort -m64

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64

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Peak Portability Flags (Continued)

631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/home/cpu2017/je5.0.1-64/ -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

623.xalancbmk_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6128 3.40 GHz)

SPEC speed2017_int_base = 8.57
SPEC speed2017_int_peak = 8.80

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Peak Optimization Flags (Continued)

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:
-W1, -z, muldefs -XCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L /home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml