## SPEC® CPU2017 Integer Speed Result

### Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6130 2.10 GHz)

<table>
<thead>
<tr>
<th>SPECspeed2017_int_base</th>
<th>8.83</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

**Test Date:** Dec-2018

### Hardware
- **CPU Name:** Intel Xeon Gold 6130
- **Max MHz.:** 3700
- **Nominal:** 2100
- **Enabled:** 64 cores, 4 chips
- **Orderable:** 2,4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 22 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 1 TB HDD, 7.2K RPM
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **Compiler:** C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.1.3e released Jun-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1

### Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>64</td>
<td>6.27</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>64</td>
<td>9.20</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>64</td>
<td>10.9</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>64</td>
<td>6.07</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>64</td>
<td>9.55</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>64</td>
<td>4.37</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>64</td>
<td>5.08</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>64</td>
<td>11.5</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>64</td>
<td>13.3</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>64</td>
<td>23.3</td>
</tr>
</tbody>
</table>

---

**SPECspeed2017_int_base (8.83)**
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6130 2.10 GHz)

SPEC CPU2017 Integer Speed Result
Copyright 2017-2018 Standard Performance Evaluation Corporation

SPECspeed2017_int_base = 8.83
SPECspeed2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
<th>Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>64</td>
<td>286</td>
<td>6.21</td>
<td>283</td>
<td>6.27</td>
<td>282</td>
<td>6.29</td>
<td></td>
<td></td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>64</td>
<td>433</td>
<td>9.21</td>
<td>434</td>
<td>9.17</td>
<td>433</td>
<td>9.20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>64</td>
<td>433</td>
<td>10.9</td>
<td>435</td>
<td>10.9</td>
<td>436</td>
<td>10.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>64</td>
<td>284</td>
<td>5.75</td>
<td>260</td>
<td>6.27</td>
<td>269</td>
<td>6.07</td>
<td></td>
<td></td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>64</td>
<td>148</td>
<td>9.55</td>
<td>150</td>
<td>9.43</td>
<td>148</td>
<td>9.57</td>
<td></td>
<td></td>
</tr>
<tr>
<td>625.x264_s</td>
<td>64</td>
<td>153</td>
<td>11.5</td>
<td>153</td>
<td>11.5</td>
<td>153</td>
<td>11.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>64</td>
<td>282</td>
<td>5.08</td>
<td>282</td>
<td>5.09</td>
<td>282</td>
<td>5.08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>641.leela_s</td>
<td>64</td>
<td>390</td>
<td>4.37</td>
<td>390</td>
<td>4.37</td>
<td>390</td>
<td>4.37</td>
<td></td>
<td></td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>64</td>
<td>221</td>
<td>13.3</td>
<td>221</td>
<td>13.3</td>
<td>221</td>
<td>13.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>64</td>
<td>265</td>
<td>23.3</td>
<td>265</td>
<td>23.3</td>
<td>266</td>
<td>23.3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
SPEC CPU2017 Integer Speed Result

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6130 2.10 GHz)

SPECspeed2017_int_base = 8.83
SPECspeed2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2018
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Mar-2018

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bdc091c0f
running on linux-9r4j Wed Dec 5 18:20:58 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
  4 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 16
  siblings: 16
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
Stepping: 4
CPU MHz: 1749.679
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4195.44
Virtualization: VT-x

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6130 2.10 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

SPECspeed2017_int_base = 8.83
SPECspeed2017_int_peak = Not Run

Platform Notes (Continued)

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>22528K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-15</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>16-31</td>
</tr>
<tr>
<td>NUMA node2 CPU(s):</td>
<td>32-47</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
<td>48-63</td>
</tr>
<tr>
<td>Flags:</td>
<td>fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp lm constant_tsc arch_perfmon pebs bts rep_good nop1 xtopology nonstop_tsc aperf mp Leaving eagerfpu pni pclmulqdq dtexec monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpcr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_cxsw spec_ctrl stibp retpoline kaiser tpr_shadow vmmi flexpriority ept vpid fsbsegbase tsc_adjust bni hle avx2 smep bmi2 3ms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsaves v xgetbv1 cqm_llc cqm_occup_llc</td>
</tr>
</tbody>
</table>

/proc/cpuinfo cache data
  cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  node 0 size: 385622 MB
  node 0 free: 385260 MB
  node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
  node 1 size: 387057 MB
  node 1 free: 386644 MB
  node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
  node 2 size: 387057 MB
  node 2 free: 386845 MB
  node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
  node 3 size: 387054 MB
  node 3 free: 386853 MB
  node distances:
    node 0 1 2 3
    0: 10 21 21 21
    1: 21 10 21 21
    2: 21 21 10 21
    3: 21 21 21 10

From /proc/meminfo
  MemTotal: 1583914512 kB
  HugePages_Total: 0

(Continued on next page)
**Cisco Systems**

Cisco UCS C480 M5 (Intel Xeon Gold 6130 2.10 GHz)

<table>
<thead>
<tr>
<th>SPECspeed2017_int_base</th>
<th>8.83</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2018</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2018</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

```
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-9r4j 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Oct 27 08:30

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used Avail Use% Mounted on
  /dev/sda1    xfs   930G  246G  685G  27% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018
Memory:
  48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)
```

**Compiler Version Notes**

```
==============================================================================
CC  600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base)
  657.xz_s(base)
==============================================================================
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6130 2.10 GHz)

SPEC CPU2017 Integer Speed Result

<table>
<thead>
<tr>
<th>SPECspeed2017_int_base</th>
<th>8.83</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Compiler Version Notes (Continued)

------------------------------------------------------------------------------
CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
641.leela_s(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
FC 648.exchange2_s(base)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
## SPEC CPU2017 Integer Speed Result

**Cisco Systems**  
Cisco UCS C480 M5 (Intel Xeon Gold 6130 2.10 GHz)

<table>
<thead>
<tr>
<th>SPECspeed2017_int_base</th>
<th>8.83</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Date:** Dec-2018  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

### Base Optimization Flags

#### C benchmarks:
- `-Wl,-z,muldefs`  
- `-xCORE-AVX512`  
- `-ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=3 `  
- `-qopenmp -DSPEC_OPENMP`  
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

#### C++ benchmarks:
- `-Wl,-z,muldefs`  
- `-xCORE-AVX512`  
- `-ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=3 `-L/usr/local/je5.0.1-64/lib -ljemalloc`

#### Fortran benchmarks:
- `-Wl,-z,muldefs`  
- `-xCORE-AVX512`  
- `-ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=3 -nostandard-realloc-lhs`  
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

The flags files that were used to format this result can be browsed at  

You can also download the XML flags sources by saving the following links:  

---

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2018-12-05 18:20:58-0500.  
Report generated on 2018-12-26 13:07:03 by CPU2017 PDF formatter v6067.  
Originally published on 2018-12-25.