**Cisco Systems**
Cisco UCS B480 M5 (Intel Xeon Gold 6138 2.00 GHz)

SPEC® CPU2017 Integer Speed Result

<table>
<thead>
<tr>
<th>Software Availability</th>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
<th>Test Date</th>
<th>CPU2017 License</th>
</tr>
</thead>
</table>

### SPECspeed2017_int_base
8.90

### SPECspeed2017_int_peak
9.18

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed2017_int_base</th>
<th>SPECspeed2017_int_peak</th>
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<tbody>
<tr>
<td>600.perlbench_s 80</td>
<td>6.25</td>
<td>7.32</td>
</tr>
<tr>
<td>602.gcc_s 80</td>
<td>9.12</td>
<td>9.32</td>
</tr>
<tr>
<td>605.mcf_s 80</td>
<td>6.53</td>
<td>10.9</td>
</tr>
<tr>
<td>620.omnetpp_s 80</td>
<td>6.84</td>
<td>11.1</td>
</tr>
<tr>
<td>623.xalancbmk_s 80</td>
<td>9.52</td>
<td>10.1</td>
</tr>
<tr>
<td>625.x264_s 80</td>
<td>10.1</td>
<td>11.6</td>
</tr>
<tr>
<td>631.deepsjeng_s 80</td>
<td>5.09</td>
<td>5.02</td>
</tr>
<tr>
<td>641.leela_s 80</td>
<td>4.38</td>
<td>4.35</td>
</tr>
<tr>
<td>648.exchange2_s 80</td>
<td>13.3</td>
<td>13.5</td>
</tr>
<tr>
<td>657.xz_s 80</td>
<td>23.8</td>
<td>24.3</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name**: Intel Xeon Gold 6138
- **Max MHz.**: 3700
- **Nominal**: 2000
- **Enabled**: 80 cores, 4 chips
- **Orderable**: 2,4 Chips
- **Cache L1**: 32 KB I + 32 KB D on chip per core
- **L2**: 1 MB I+D on chip per core
- **L3**: 27.5 MB I+D on chip per chip
- **Other**: None
- **Memory**: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
- **Storage**: 1 x 400 GB SSD SAS
- **Other**: None

**Software**

- **OS**: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
- **Compiler**: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
- **Parallel**: Yes
- **Firmware**: Version 3.2.3c released Mar-2018
- **File System**: xfs
- **System State**: Run level 3 (multi-user)
- **Base Pointers**: 64-bit
- **Peak Pointers**: 32/64-bit
- **Other**: jemalloc memory allocator V5.0.1
## SPEC CPU2017 Integer Speed Result

**Cisco Systems**  
Cisco UCS B480 M5 (Intel Xeon Gold 6138 2.00 GHz)  

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<td><strong>Tested by:</strong></td>
<td>Cisco Systems</td>
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### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
<th>Seconds</th>
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<th>Ratio</th>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>80</td>
<td>283</td>
<td>6.27</td>
<td>284</td>
<td>6.25</td>
<td>287</td>
<td>6.18</td>
<td>80</td>
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<td>7.45</td>
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<td>7.42</td>
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<td>620.omnetpp_s</td>
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<td>149</td>
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<td>9.41</td>
<td>149</td>
<td>9.53</td>
<td>80</td>
<td>140</td>
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<td>139</td>
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<td>140</td>
<td>10.1</td>
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<tr>
<td>625.x264_s</td>
<td>80</td>
<td>152</td>
<td>11.6</td>
<td>152</td>
<td>11.6</td>
<td>152</td>
<td>11.6</td>
<td>80</td>
<td>152</td>
<td>11.6</td>
<td>153</td>
<td>11.5</td>
<td>152</td>
<td>11.6</td>
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<tr>
<td>631.deepsjeng_s</td>
<td>80</td>
<td>282</td>
<td>5.08</td>
<td>281</td>
<td>5.10</td>
<td>282</td>
<td>5.09</td>
<td>80</td>
<td>285</td>
<td>5.03</td>
<td>286</td>
<td>5.02</td>
<td>286</td>
<td>5.02</td>
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<tr>
<td>641.leela_s</td>
<td>80</td>
<td>390</td>
<td>4.38</td>
<td>390</td>
<td>4.37</td>
<td>390</td>
<td>4.38</td>
<td>80</td>
<td>392</td>
<td>4.35</td>
<td>392</td>
<td>4.35</td>
<td>393</td>
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<tr>
<td>648.exchange2_s</td>
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<td>222</td>
<td>13.3</td>
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<td>80</td>
<td>217</td>
<td>13.5</td>
<td>218</td>
<td>13.5</td>
<td>218</td>
<td>13.5</td>
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<tr>
<td>657.xz_s</td>
<td>80</td>
<td>257</td>
<td>24.0</td>
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<td>260</td>
<td>23.7</td>
<td>80</td>
<td>255</td>
<td>24.3</td>
<td>257</td>
<td>24.0</td>
<td>255</td>
<td>24.3</td>
</tr>
</tbody>
</table>

**SPECspeed2017_int_base = 8.90**  
**SPECspeed2017_int_peak = 9.18**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### General Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3 > /proc/sys/vm/drop_caches  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.  
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6138 2.00 GHz)

SPEC CPU2017 Integer Speed Result

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SPECspeed2017_int_base = 8.90
SPECspeed2017_int_peak = 9.18

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bacc091c0f
running on linux-xy4f Thu Nov 29 17:31:23 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6138 CPU @ 2.00GHz
  4 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 2: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 3: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 1
Core(s) per socket: 20
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6138 CPU @ 2.00GHz
Stepping: 4
CPU MHz: 1111.156
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 3999.97
Virtualization: VT-x

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6138 2.00 GHz)

SPEC CPU2017 Integer Speed Result

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SPECspeed2017_int_base = 8.90
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39
NUMA node2 CPU(s): 40-59
NUMA node3 CPU(s): 60-79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmon perf eagerpfn pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat ept vpd invpcid_single pln pts
dtherm hwlp act_window hwp_epp hwp_pkg_req intel_pt rsbمراقب spec ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 3dnow invpcid rtm cqm mpx avx512f avx512d rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup LLC

/proc/cpuinfo cache data
cache size : 28160 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
cache size : 28160 KB

physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
node 0 size: 385624 MB
node 0 free: 385314 MB
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
node 1 size: 387057 MB
node 1 free: 386780 MB
node 2 cpus: 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59
node 2 size: 387057 MB
node 2 free: 386816 MB
node 3 cpus: 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
node 3 size: 387054 MB
node 3 free: 386876 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

From /proc/meminfo
MemTotal: 1583916132 kB
HugePages_Total: 0

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Cisco Systems
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</tbody>
</table>

### Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

SuSE-release:
- SUSE Linux Enterprise Server 12 (x86_64)
- VERSION = 12
- PATCHLEVEL = 2

# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

os-release:
- NAME="SLES"
- VERSION="12-SP2"
- VERSION_ID="12.2"
- PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
- ID="sles"
- ANSI_COLOR="0;32"
- CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
- Linux linux-xy4f 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
- x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 31 19:06

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda1</td>
<td>xfs</td>
<td>224G</td>
<td>70G</td>
<td>154G</td>
<td>32%</td>
<td>/</td>
</tr>
</tbody>
</table>

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018

Memory:
- 48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

### Compiler Version Notes

==============================================================================
| CC 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base, peak) 657.xz_s(base) |
==============================================================================

icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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## Cisco Systems

**Cisco UCS B480 M5 (Intel Xeon Gold 6138 2.00 GHz)**

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</tbody>
</table>

**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

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### Compiler Version Notes (Continued)

```plaintext
CC  600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
---
ICC (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
641.leela_s(base)
---
ICPC (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

CXXC 620.omnetpp_s(peak) 623.xalancbmk_s(peak) 631.deepsjeng_s(peak)
641.leela_s(peak)
---
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

FC 648.exchange2_s(base, peak)
---
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---
```

---

### Base Compiler Invocation

**C benchmarks:**  
```bash
icc -m64 -std=c11
```  
**C++ benchmarks:**  
```bash
icpc -m64
```  
**Fortran benchmarks:**  
```bash
ifort -m64
```
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6138 2.00 GHz)

SPECspeed2017_int_base = 8.90
SPECspeed2017_int_peak = 9.18

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Base Portability Flags
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Compiler Invocation
C benchmarks:
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64

623.xalancbmk_s: icpc -m32 -L/home/prasadj/specdev/IC18u2_Internal/lin_18_0_20180210/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64
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Cisco UCS B480 M5 (Intel Xeon Gold 6138 2.00 GHz)

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SPECspeed2017_int_peak = 9.18

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-prefetch -ipo -O3
-qopt-mem-layout-trans=3 -no-prec-div
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib
-ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-prefetch -ipo -O3
-qopt-mem-layout-trans=3 -no-prec-div
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp

C++ benchmarks:

620.omnetpp_p_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp

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SPEC CPU2017 Integer Speed Result

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SPECspeed2017_int_base = 8.90
SPECspeed2017_int_peak = 9.18

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Peak Optimization Flags (Continued)

620.omnetpp_s (continued):
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

623.xalancbmk_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-32/lib -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s
641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-L/usr/local/je5.0.1-64/lib -ljemalloc

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

The flags files that were used to format this result can be browsed at

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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