## SPEC® CPU2017 Integer Speed Result

**Cisco Systems**

Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)

<table>
<thead>
<tr>
<th>SPECspeed2017_int_base</th>
<th>8.81</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_peak</td>
<td>9.00</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6130
- **Max MHz.:** 3700
- **Nominal:** 2100
- **Enabled:** 64 cores, 4 chips
- **Orderable:** 2,4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 400 GB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
- **Compiler:** C/C++: Version 18.0.2.199 of Intel C/C++
- **Compiler for Linux:** Fortran: Version 18.0.2.199 of Intel Fortran
- **Compiler for Linux:**
- **Firmware:** Yes
- **Firmware:** Version 3.2.3c released Mar-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1

### Benchmarks

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed2017_int_base</th>
<th>SPECspeed2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_s</td>
<td>64</td>
<td>6.16</td>
<td>7.31</td>
</tr>
<tr>
<td>gcc_s</td>
<td>64</td>
<td>9.04</td>
<td>9.20</td>
</tr>
<tr>
<td>mcf_s</td>
<td>64</td>
<td>8.19</td>
<td>11.0</td>
</tr>
<tr>
<td>omnetpp_s</td>
<td>64</td>
<td>5.82</td>
<td>10.1</td>
</tr>
<tr>
<td>xalancbmk_s</td>
<td>64</td>
<td>9.49</td>
<td>11.5</td>
</tr>
<tr>
<td>x264_s</td>
<td>64</td>
<td>5.09</td>
<td>11.5</td>
</tr>
<tr>
<td>deepsjeng_s</td>
<td>64</td>
<td>5.02</td>
<td>13.3</td>
</tr>
<tr>
<td>leela_s</td>
<td>64</td>
<td>4.37</td>
<td>13.5</td>
</tr>
<tr>
<td>exchange2_s</td>
<td>64</td>
<td>6.19</td>
<td>23.3</td>
</tr>
<tr>
<td>xz_s</td>
<td>64</td>
<td>5.82</td>
<td>23.5</td>
</tr>
</tbody>
</table>

**Test Sponsor:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018
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**SPECspeed2017_int_base = 8.81**  
**SPECspeed2017_int_peak = 9.00**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>64</td>
<td>284</td>
<td>6.26</td>
<td>288</td>
<td>6.16</td>
<td>288</td>
<td>6.16</td>
<td>64</td>
<td>241</td>
<td>7.36</td>
<td>243</td>
<td>7.31</td>
<td>248</td>
<td>7.16</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>64</td>
<td>442</td>
<td>9.02</td>
<td>439</td>
<td>9.06</td>
<td>441</td>
<td>9.04</td>
<td>64</td>
<td>430</td>
<td>9.25</td>
<td>433</td>
<td>9.19</td>
<td>433</td>
<td>9.20</td>
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<tr>
<td>605.mcf_s</td>
<td>64</td>
<td>433</td>
<td>10.9</td>
<td>431</td>
<td>11.0</td>
<td>431</td>
<td>11.0</td>
<td>64</td>
<td>429</td>
<td>11.0</td>
<td>429</td>
<td>11.0</td>
<td>428</td>
<td>11.0</td>
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<tr>
<td>620.omnetpp_s</td>
<td>64</td>
<td>261</td>
<td>6.25</td>
<td>293</td>
<td>5.56</td>
<td>263</td>
<td>6.19</td>
<td>64</td>
<td>272</td>
<td>5.99</td>
<td>280</td>
<td>5.82</td>
<td>291</td>
<td>5.61</td>
</tr>
<tr>
<td>623.xalancmk_s</td>
<td>64</td>
<td>149</td>
<td>9.48</td>
<td>149</td>
<td>9.49</td>
<td>147</td>
<td>9.61</td>
<td>64</td>
<td>140</td>
<td>10.1</td>
<td>140</td>
<td>10.1</td>
<td>140</td>
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<tr>
<td>625.x264_s</td>
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<td>154</td>
<td>11.5</td>
<td>153</td>
<td>11.5</td>
<td>153</td>
<td>11.5</td>
<td>64</td>
<td>153</td>
<td>11.5</td>
<td>153</td>
<td>11.5</td>
<td>153</td>
<td>11.5</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>64</td>
<td>282</td>
<td>5.09</td>
<td>282</td>
<td>5.09</td>
<td>282</td>
<td>5.08</td>
<td>64</td>
<td>286</td>
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<td>285</td>
<td>5.02</td>
<td>286</td>
<td>5.02</td>
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<tr>
<td>641.leela_s</td>
<td>64</td>
<td>390</td>
<td>4.38</td>
<td>390</td>
<td>4.37</td>
<td>390</td>
<td>4.37</td>
<td>64</td>
<td>393</td>
<td>4.34</td>
<td>392</td>
<td>4.35</td>
<td>392</td>
<td>4.35</td>
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<tr>
<td>648.exchange2_s</td>
<td>64</td>
<td>222</td>
<td>13.3</td>
<td>221</td>
<td>13.3</td>
<td>222</td>
<td>13.3</td>
<td>64</td>
<td>217</td>
<td>13.6</td>
<td>218</td>
<td>13.5</td>
<td>218</td>
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<tr>
<td>657.xz_s</td>
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<td>266</td>
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<td>265</td>
<td>23.3</td>
<td>266</td>
<td>23.2</td>
<td>64</td>
<td>263</td>
<td>23.5</td>
<td>263</td>
<td>23.5</td>
<td>260</td>
<td>23.8</td>
</tr>
</tbody>
</table>

---

### Results Table

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
```
  sync; echo 3> /proc/sys/vm/drop_caches
```
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)  
is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)  
is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)  
is mitigated in the system as tested and documented.  
jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
## SPEC CPU2017 Integer Speed Result

### Cisco Systems

**Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

**SPECspeed2017_int_base = 8.81**

**SPECspeed2017_int_peak = 9.00**

---

### Platform Notes

**BIOS Settings:**
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- Patrol Scrub set to Disabled
- Sysinfo program `/home/cpu2017/bin/sysinfo`
  - Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
  - Running on `linux-xy4f Fri Nov 30 20:41:09 2018`

**SUT (System Under Test) info as seen by some common utilities.**

For more information on this section, see

https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From `/proc/cpuinfo`

- `model name`: Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
- `cpu cores`: 16
- `siblings`: 16
  - physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From `lscpu`:

- `Architecture`: x86_64
- `CPU op-mode(s)`: 32-bit, 64-bit
- `Byte Order`: Little Endian
- `CPU(s)`: 64
- `On-line CPU(s) list`: 0-63
- `Thread(s) per core`: 1
- `Core(s) per socket`: 16
- `Socket(s)`: 4
- `NUMA node(s)`: 4
- `Vendor ID`: GenuineIntel
- `CPU family`: 6
- `Model`: 85
- `Model name`: Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
- `Stepping`: 4
- `CPU MHz`: 1148.930
- `CPU max MHz`: 3700.0000
- `CPU min MHz`: 1000.0000
- `BogoMIPS`: 4199.98
- `Virtualization`: VT-x

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)

SPECcpu2017 Integer Speed Result

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SPECspeed2017_int_peak = 9.00
SPECspeed2017_int_base = 8.81

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

<table>
<thead>
<tr>
<th>cache</th>
<th>size</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>22528K</td>
</tr>
</tbody>
</table>

NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
NUMA node2 CPU(s): 32-47
NUMA node3 CPU(s): 48-63

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good ntopology nonstop_tsc
aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcz pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxtsw spec_ctrl stibp
retpoline kaiser tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavevc xsaves vsgetbv1 cqm_llc cqm_occuv_llc

/proc/cpuinfo cache data

| cache size | 22528 KB |

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

<table>
<thead>
<tr>
<th>available</th>
<th>4 nodes (0-3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>node 0 cpus: 0</td>
<td>1 2 3 4 5 6 7 8 9 10 11 12 13 14 15</td>
</tr>
<tr>
<td>node 0 size:</td>
<td>385624 MB</td>
</tr>
<tr>
<td>node 0 free:</td>
<td>385294 MB</td>
</tr>
<tr>
<td>node 1 cpus: 16</td>
<td>17 18 19 20 21 22 23 24 25 26 27 28 29 30 31</td>
</tr>
<tr>
<td>node 1 size:</td>
<td>387057 MB</td>
</tr>
<tr>
<td>node 1 free:</td>
<td>386829 MB</td>
</tr>
<tr>
<td>node 2 cpus: 32</td>
<td>33 34 35 36 37 38 39 40 41 42 43 44 45 46 47</td>
</tr>
<tr>
<td>node 2 size:</td>
<td>387057 MB</td>
</tr>
<tr>
<td>node 2 free:</td>
<td>386829 MB</td>
</tr>
<tr>
<td>node 3 cpus: 48</td>
<td>49 50 51 52 53 54 55 56 57 58 59 60 61 62 63</td>
</tr>
<tr>
<td>node 3 size:</td>
<td>387054 MB</td>
</tr>
<tr>
<td>node 3 free:</td>
<td>386864 MB</td>
</tr>
</tbody>
</table>

node distances:

<table>
<thead>
<tr>
<th>node 0 1 2 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0: 10 21 21 21</td>
</tr>
<tr>
<td>1: 21 10 21 21</td>
</tr>
<tr>
<td>2: 21 21 10 21</td>
</tr>
<tr>
<td>3: 21 21 21 10</td>
</tr>
</tbody>
</table>

From /proc/meminfo

| MemTotal: | 1583916196 kB |
| HugePages_Total: | 0 |

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz) SPECspeed2017_int_base = 8.81 SPECspeed2017_int_peak = 9.00

CPU2017 License: 9019 Test Date: Nov-2018
Test Sponsor: Cisco Systems Hardware Availability: Aug-2017
Tested by: Cisco Systems Software Availability: Mar-2018

Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*

SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.

os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PATCHLEVEL=2
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-xy4f 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 31 19:05

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 70G 154G 32% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
Memory:
  48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

========================================================================================================
CC  600.perlibench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base,peak) 657.xz_s(base)
========================================================================================================

icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)

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Compiler Version Notes (Continued)

Compiler Version Notes (Continued)

---

CC  600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
iccc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
641.leela_s(base)
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

CXXC 620.omnetpp_s(peak) 623.xalancbmk_s(peak) 631.deepsjeng_s(peak)
641.leela_s(peak)
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

FC 648.exchange2_s(base, peak)
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

Base Compiler Invocation

Base Compiler Invocation

---

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64
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Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64

623.xalancbmk_s: icpc -m32 -L/home/prasadj/specdev/IC18u2_Internal/lin_18_0_20180210/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)

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** SPECspeed2017_int_peak = 9.00 **

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Nov-2018  
Hardware Availability: Aug-2017  
Software Availability: Mar-2018

---

** Peak Portability Flags **

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
602.gcc_s: -DSPEC_LP64  
605.mcf_s: -DSPEC_LP64  
620.omnetpp_s: -DSPEC_LP64  
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
625.x264_s: -DSPEC_LP64  
631.deepsjeng_s: -DSPEC_LP64  
641.leela_s: -DSPEC_LP64  
648.exchange2_s: -DSPEC_LP64  
657.xz_s: -DSPEC_LP64

---

** Peak Optimization Flags **

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-prefetch -ipo -O3  
-qopt-mem-layout-trans=3 -no-prec-div  
-DSPEC.SuppressOpenMP -qopenmp -DSPEC.OpenMP  
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib  
-ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-prefetch -ipo -O3  
-qopt-mem-layout-trans=3 -no-prec-div  
-DSPEC.SuppressOpenMP -qopenmp -DSPEC.OpenMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch  
-qopt-mem-layout-trans=3 -DSPEC.SuppressOpenMP -qopenmp  
-DSPEC.OpenMP -L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-prefetch -qopt-mem-layout-trans=3 -qopenmp  
-DSPEC.OpenMP -L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch  
-qopt-mem-layout-trans=3 -DSPEC.SuppressOpenMP -qopenmp

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)

<table>
<thead>
<tr>
<th>SPEC CPU2017 Integer Speed Result</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SPECspeed2017_int_base</strong> = 8.81</td>
</tr>
<tr>
<td><strong>SPECspeed2017_int_peak</strong> = 9.00</td>
</tr>
</tbody>
</table>

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

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**Peak Optimization Flags (Continued)**

620.omnetpp_s (continued):
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

623.xalancbmk_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch  
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -L/usr/local/je5.0.1-32/lib -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

For Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs  
-L/usr/local/je5.0.1-64/lib -ljemalloc

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The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml  
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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