## SPEC® CPU2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed2017_fp_base =</th>
<th>SPECspeed2017_fp_peak =</th>
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<tbody>
<tr>
<td>603.bwaves_s 64</td>
<td>149</td>
<td>Not Run</td>
</tr>
<tr>
<td>607.cactuBSSN_s 64</td>
<td></td>
<td></td>
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<tr>
<td>619.lbm_s 64</td>
<td>40.0</td>
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<tr>
<td>621.wrf_s 64</td>
<td>111</td>
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<tr>
<td>627.cam4_s 64</td>
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<tr>
<td>628.pop2_s 64</td>
<td>115</td>
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<td>638.imagick_s 64</td>
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<td>644.nab_s 64</td>
<td>319</td>
<td></td>
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<tr>
<td>649.fotonik3d_s 64</td>
<td>235</td>
<td></td>
</tr>
<tr>
<td>654.roms_s 64</td>
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</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6130
- **Max MHz.:** 3700
- **Nominal:** 2100
- **Enabled:** 64 cores, 4 chips
- **Orderable:** 2,4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 400 GB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **Compiler:** C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.2.3c released Mar-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
SPEC CPU2017 Floating Point Speed Result

Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Specspeed2017_fp_base = 149
Specspeed2017_fp_peak = Not Run

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Results Table

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<td>644.nab_s</td>
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<tr>
<td>654.roms_s</td>
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<td>67.2</td>
<td>234</td>
<td>66.6</td>
<td>236</td>
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</tr>
</tbody>
</table>

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-xy4f Sat Dec 1 01:46:45 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```plaintext
model name : Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
  4 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu:

```plaintext
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
Stepping: 4
CPU MHz: 1410.835
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4199.98
Virtualization: VT-x
```

(Continued on next page)
### Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Platform Notes</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>L1d cache:</strong></td>
<td>32K</td>
</tr>
<tr>
<td><strong>L1i cache:</strong></td>
<td>32K</td>
</tr>
<tr>
<td><strong>L2 cache:</strong></td>
<td>1024K</td>
</tr>
<tr>
<td><strong>L3 cache:</strong></td>
<td>22528K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-15</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>16-31</td>
</tr>
<tr>
<td>NUMA node2 CPU(s):</td>
<td>32-47</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
<td>48-63</td>
</tr>
<tr>
<td><strong>Flags:</strong></td>
<td>fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp retropoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc</td>
</tr>
</tbody>
</table>

```
/proc/cpuinfo cache data
  cache size : 22528 KB
```

From `numactl --hardware` WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385624 MB
node 0 free: 384384 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387057 MB
node 1 free: 384291 MB
node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 2 size: 387057 MB
node 2 free: 385708 MB
node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
node 3 size: 387054 MB
node 3 free: 384344 MB
node distances:
  node 0 1 2 3
  0: 10 21 21 21
  1: 21 10 21 21
  2: 21 21 10 21
  3: 21 21 21 10
```

From `/proc/meminfo`

```
MemTotal: 1583916196 kB
HugePages_Total: 0
```

(Continued on next page)
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SPECspeed2017_fp_base = 149
SPECspeed2017_fp_peak = Not Run

CPU2017 License: 9019
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Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-xy4f 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 31 19:05

SPEC is set to: /home/cpu2017
  filesystem type size used avail use% mounted on
  /dev/sda1 xfs 224G 76G 148G 34% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
  Memory:
    48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
==============================================================================
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)

SPEC CPU2017 Floating Point Speed Result
Copyright 2017-2018 Standard Performance Evaluation Corporation

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Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Compiler Version Notes (Continued)

==============================================================================
FC  607.cactuBSSN_s(base)
------------------------------------------------------------------------------
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
FC  603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
CC  621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64
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Cisco UCS B480 M5 (Intel Xeon Gold 6130 2.10 GHz)

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### Base Portability Flags

- 603.bwaves_s: -DSPEC_LP64
- 607.cactuBSSN_s: -DSPEC_LP64
- 619.ibm_s: -DSPEC_LP64
- 621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
- 638.imagick_s: -DSPEC_LP64
- 644.nab_s: -DSPEC_LP64
- 649.fotonik3d_s: -DSPEC_LP64
- 654.roms_s: -DSPEC_LP64

### Base Optimization Flags

#### C benchmarks:

- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

#### Fortran benchmarks:

- Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -L/usr/local/je5.0.1-64/lib -ljemalloc

#### Benchmarks using both Fortran and C:

- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -L/usr/local/je5.0.1-64/lib -ljemalloc

#### Benchmarks using Fortran, C, and C++:

- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -L/usr/local/je5.0.1-64/lib -ljemalloc

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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