## SPEC® CPU2017 Integer Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Silver 4110 2.10 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Dec-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Oct-2018</td>
</tr>
</tbody>
</table>

### CPU2017 License:
- 9019

### Hardware

**CPU Name:** Intel Xeon Silver 4110  
**Max MHz.:** 3000  
**Nominal:** 2100  
**Enabled:** 16 cores, 2 chips, 2 threads/core  
**Orderable:** 1,2 Chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 11 MB I+D on chip per chip  
**Other:** None  
**Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)  
**Storage:** 1 x 400 GB SAS SSD  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)  
**Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;  
**Compiler for Linux:** Fortran: Version 19.0.1.144 of Intel Fortran  
**Compiler for Linux:**  
**Parallel:** No  
**Firmware:** Version 4.0.1 released Oct-2018  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 32/64-bit  
**Other:** jemalloc memory allocator V5.0.1

### SPECrate2017 int_base = 73.3

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate2017 int_peak</th>
<th>SPECrate2017 int_base</th>
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</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>32</td>
<td>57.2</td>
<td>63.3</td>
</tr>
<tr>
<td>gcc</td>
<td>32</td>
<td>68.3</td>
<td></td>
</tr>
<tr>
<td>mcf</td>
<td>32</td>
<td>47.3</td>
<td></td>
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<tr>
<td>omnetpp</td>
<td>32</td>
<td>71.4</td>
<td></td>
</tr>
<tr>
<td>xalancbmk</td>
<td>32</td>
<td>87.7</td>
<td></td>
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<tr>
<td>x264</td>
<td>32</td>
<td>65.0</td>
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<td>deepsjeng</td>
<td>32</td>
<td>64.4</td>
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<td>leela</td>
<td>32</td>
<td>59.7</td>
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<tr>
<td>exchange2</td>
<td>32</td>
<td>136</td>
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<tr>
<td>xz</td>
<td>32</td>
<td>53.5</td>
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SPECrate2017_int_base = 73.3
SPECrate2017_int_peak = 78.2

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>903</td>
<td>56.4</td>
<td>889</td>
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<td>502.gcc_r</td>
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<td>505.mcf_r</td>
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<td>520.omnetpp_r</td>
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<td>883</td>
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<td>541.leela_r</td>
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<tr>
<td>557.xz_r</td>
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<td>646</td>
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<td>644</td>
<td>53.6</td>
<td>645</td>
<td>53.6</td>
</tr>
</tbody>
</table>

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Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4110 2.10 GHz)

SPECrater2017_int_base = 73.3
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Hardware Availability: Aug-2017
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General Notes (Continued)

ejemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-yoo1 Tue Dec 18 09:48:54 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz

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<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Stepping</td>
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<tr>
<td>CPU MHz</td>
<td>1680.613</td>
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<tr>
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<tr>
<td>CPU min MHz</td>
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<td>BogoMIPS</td>
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<td>Virtualization</td>
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<tr>
<td>L1d cache</td>
<td>32K</td>
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<td>L1i cache</td>
<td>32K</td>
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<td>L2 cache</td>
<td>1024K</td>
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<tr>
<td>L3 cache</td>
<td>11264K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s)</td>
<td>0-7,16-23</td>
</tr>
<tr>
<td>NUMA node1 CPU(s)</td>
<td>8-15,24-31</td>
</tr>
<tr>
<td>Flags</td>
<td>fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp l m constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts dtherm hwlp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp retpoline kaiser tpr_shadow vmmi flexpriority ept vpid fsblsparce tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cmp mp{x avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc</td>
</tr>
</tbody>
</table>

/proc/cpuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

From /proc/meminfo
MemTotal:    792192220 kB
HugePages_Total:   0
Hugepagesize:  2048 kB

From /etc/*release* /etc/*version*
SuSE-release:

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Tested by: Cisco Systems
Software Availability: Oct-2018

Platform Notes (Continued)

SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-yoo1 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 17 15:46

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda1      xfs   224G  121G  104G  54% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
Memory:
  12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400
  12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
    525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================

icc (ICC) 19.0.1.144 20181018
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==============================================================================
(Continued on next page)
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Cisco UCS C240 M5 (Intel Xeon Silver 4110 2.10 GHz)

SPEC CPU2017 Integer Rate Result

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Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

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### Base Portability Flags (Continued)

502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

**C++ benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

**Fortran benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
- -L/home/cpu2017/je5.0.1-64/ -ljemalloc

### Peak Compiler Invocation

**C benchmarks (except as noted below):**
- icc -m64 -std=c11
- 502.gcc_r: icc -m32 -std=c11 -L/opt/intel/lib/ia32

**C++ benchmarks (except as noted below):**
- icpc -m64
- 523.xalancbmk_r: icpc -m32 -L/opt/intel/lib/ia32

**Fortran benchmarks:**
- ifort -m64
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Cisco UCS C240 M5 (Intel Xeon Silver 4110 2.10 GHz)

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Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/home/cpu2017/je5.0.1-64/
-ljemalloc
502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/
-ljemalloc
525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
557.xz_r: Same as 505.mcf_r

C++ benchmarks:
520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

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Cisco Systems

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| SPECrate2017_int_base | 73.3 |
| SPECrate2017_int_peak | 78.2 |

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Test Sponsor: Cisco Systems
Tested by: Cisco Systems

**Peak Optimization Flags (Continued)**

- 531.deepsjeng_r: Same as 520.omnetpp_r
- 541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
- -L/home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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