## SPEC CPU®2017 Integer Speed Result

### Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)  

| SPECspeed®2017_int_base | 8.96  
|------------------------|------  
| SPECspeed®2017_int_peak | 9.24  

#### Hardware

| CPU Name: | Intel Xeon Gold 6142M  
| Max MHz: | 3700  
| Nominal: | 2600  
| Enabled: | 32 cores, 2 chips  
| Orderable: | 1.2 Chips  
| Cache L1: | 32 KB I + 32 KB D on chip per core  
| L2: | 1 MB I+D on chip per core  
| L3: | 22 MB I+D on chip per core  
| Other: | None  
| Memory: | 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)  
| Storage: | 1 x 600G SAS 10K RPM  
| Other: | None  

#### Software

| OS: | SUSE Linux Enterprise Server 12 SP2 (x86_64)  
| Compiler: | C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux  
| Parallel: | Yes  
| Firmware: | Version 4.0.1 released Oct-2018  
| File System: | xfs  
| System State: | Run level 3 (multi-user)  
| Base Pointers: | 64-bit  
| Peak Pointers: | 32/64-bit  
| Other: | jemalloc memory allocator V5.0.1  
| Power Management: | --  

---

**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Aug-2017  
**Test Date:** Nov-2018  
**Software Availability:** Oct-2018
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>32</td>
<td>283</td>
<td>6.27</td>
<td>285</td>
<td>6.24</td>
<td>282</td>
<td>6.30</td>
<td>32</td>
<td>238</td>
<td>7.47</td>
<td>236</td>
<td>7.51</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>32</td>
<td>426</td>
<td>11.1</td>
<td>426</td>
<td>11.1</td>
<td>427</td>
<td>11.1</td>
<td>32</td>
<td>425</td>
<td>11.1</td>
<td>425</td>
<td>11.1</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>32</td>
<td>272</td>
<td>6.00</td>
<td>272</td>
<td>5.99</td>
<td>268</td>
<td>6.10</td>
<td>32</td>
<td>263</td>
<td>6.19</td>
<td>262</td>
<td>6.24</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>32</td>
<td>150</td>
<td>9.44</td>
<td>150</td>
<td>9.48</td>
<td>150</td>
<td>9.47</td>
<td>32</td>
<td>138</td>
<td>10.3</td>
<td>138</td>
<td>10.2</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>32</td>
<td>135</td>
<td>13.0</td>
<td>135</td>
<td>13.0</td>
<td>135</td>
<td>13.1</td>
<td>32</td>
<td>135</td>
<td>13.0</td>
<td>135</td>
<td>13.0</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>32</td>
<td>275</td>
<td>5.22</td>
<td>275</td>
<td>5.22</td>
<td>275</td>
<td>5.22</td>
<td>32</td>
<td>278</td>
<td>5.15</td>
<td>278</td>
<td>5.16</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>32</td>
<td>377</td>
<td>4.53</td>
<td>377</td>
<td>4.53</td>
<td>377</td>
<td>4.52</td>
<td>32</td>
<td>378</td>
<td>4.52</td>
<td>378</td>
<td>4.51</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>32</td>
<td>219</td>
<td>13.4</td>
<td>219</td>
<td>13.4</td>
<td>219</td>
<td>13.4</td>
<td>32</td>
<td>220</td>
<td>13.4</td>
<td>219</td>
<td>13.4</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>32</td>
<td>283</td>
<td>21.9</td>
<td>282</td>
<td>21.9</td>
<td>282</td>
<td>21.9</td>
<td>32</td>
<td>279</td>
<td>22.1</td>
<td>281</td>
<td>22.0</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
Memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
- sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
Sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad5c135fd618bfc091c0f
running on linux-dkz7 Fri Dec 7 01:14:26 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
Stepping: 4
CPU MHz: 1344.441
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 5187.80
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECs\textsuperscript{\copyright}2017\_int\_base = 8.96
SPECs\textsuperscript{\copyright}2017\_int\_peak = 9.24

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31

Flags: fpu vme de pse sse mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_krdwr intel_pt rsb_ctxtsw spec_ctrl stibp
retpoline kaiser tpr_shadow vmvi flexpriority etptid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erts invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
c1wb avx512cf avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occullc

\texttt{/proc/cpuinfo}\ cache data
\hspace{1cm} cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
\hspace{1cm} available: 2 nodes (0-1)
\hspace{1cm} node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
\hspace{1cm} node 0 size: 385626 MB
\hspace{1cm} node 0 free: 385057 MB
\hspace{1cm} node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
\hspace{1cm} node 1 size: 387054 MB
\hspace{1cm} node 1 free: 386590 MB
\hspace{1cm} node distances:
\hspace{1cm} node 0 1
\hspace{1cm} 0: 10 21
\hspace{1cm} 1: 21 10

From /proc/meminfo
\hspace{1cm} MemTotal: 791225564 kB
\hspace{1cm} HugePages_Total: 0
\hspace{1cm} Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
\hspace{1cm} SUSE Linux Enterprise Server 12 (x86_64)
\hspace{1cm} VERSION = 12
\hspace{1cm} PATCHLEVEL = 2
\hspace{1cm} # This file is deprecated and will be removed in a future service pack or release.
\hspace{1cm} # Please check /etc/os-release for details about this release.
\hspace{1cm} os-release:
\hspace{1cm} NAME="SLES"
\hspace{1cm} VERSION="12-SP2"

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECspeed®2017_int_base = 8.96
SPECspeed®2017_int_peak = 9.24

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2018
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Oct-2018

Platform Notes (Continued)

VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 7 01:13

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 500G 118G 383G 24% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
Memory:
    12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
    12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

---------------------------------------------------------------------
C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
---------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---------------------------------------------------------------------

---------------------------------------------------------------------
C++      | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
          | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
---------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---------------------------------------------------------------------

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>8.96</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
<td>9.24</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Compiler Version Notes (Continued)

Fortran | 648.exchange2_s(base, peak)
---
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

(Continued on next page)
**Base Optimization Flags (Continued)**

Fortran benchmarks:
- `w1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`  
- `/home/cpu2017/je5.0.1-64/ -ljemalloc`

---

**Peak Compiler Invocation**

C benchmarks:
- `icc -m64 -std=c11`

C++ benchmarks (except as noted below):
- `icpc -m64`

623.xalancbmk_s: `icpc -m32 -L/opt/intel/lib/ia32`

Fortran benchmarks:
- `ifort -m64`

---

**Peak Portability Flags**

600.perlbench_s: `-DSPEC_LP64 -DSPEC_LINUX_X64`
602.gcc_s: `-DSPEC_LP64`
605.mcfs_s: `-DSPEC_LP64`
620.omnetpp_s: `-DSPEC_LP64`
623.xalancbmk_s: `-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
625.x264_s: `-DSPEC_LP64`
631.deepsjeng_s: `-DSPEC_LP64`
641.leea_s: `-DSPEC_LP64`
648.exchange2_s: `-DSPEC_LP64`
657.xz_s: `-DSPEC_LP64`

---

**Peak Optimization Flags**

C benchmarks:
- `600.perlbench_s: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`  
- `-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3`  
- `-no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp`  
- `-DSPEC_OPENMP -fno-strict-overflow`  
- `/home/cpu2017/je5.0.1-64/ -ljemalloc`

(Continued on next page)
# SPEC CPU®2017 Integer Speed Result

## Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
<th>Tested by</th>
<th>Software Availability</th>
</tr>
</thead>
</table>

### SPECspeed®2017_int_base = 8.96

### SPECspeed®2017_int_peak = 9.24

## Peak Optimization Flags (Continued)

602.gcc_s: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3 -no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMPMP -L/home/cpu2017/je5.0.1-64/ -ljemalloc

605.mcf_s: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMPMP -L/home/cpu2017/je5.0.1-64/ -ljemalloc

625.x264_s: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -gopenmp -DSPEC_OPENMPMP -L/home/cpu2017/je5.0.1-64/ -ljemalloc

657.xz_s: Same as 602.gcc_s

### C++ benchmarks:

620.omnetpp_s: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMPMP -L/home/cpu2017/je5.0.1-64/ -ljemalloc

623.xalancbmk_s: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMPMP -L/home/cpu2017/je5.0.1-32/ -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

### Fortran benchmarks:


The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml

http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECspeed®2017_int_base = 8.96
SPECspeed®2017_int_peak = 9.24

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-12-07 04:14:25-0500.
Originally published on 2019-01-29.