Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

| Copies | 0 | 3.0 | 6.0 | 9.0 | 12.0 | 15.0 | 18.0 | 21.0 | 24.0 | 27.0 | 30.0 | 33.0 | 36.0 | 39.0 | 42.0 | 45.0 | 48.0 | 51.0 | 54.0 | 57.0 | 60.0 | 63.0 | 66.0 |
|--------|---|-----|-----|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 500.perlbench_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 502.gcc_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 505.mcf_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 520.omnetpp_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 523.xalancbmk_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 525.x264_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 531.deepsjeng_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 541.leela_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 548.exchange2_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 557.zx_r | 12 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |

**Hardware**

- **CPU Name:** Intel Xeon Bronze 3104
- **Max MHz.:** 1700
- **Nominal:** 1700
- **Enabled:** 12 cores, 2 chips
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 8.25 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2133)
- **Storage:** 1 x 400 GB SAS SSD
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.1 released Oct-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1

**SPEC® CPU2017 Integer Rate Result**

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>SPECrate2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>33.4</td>
<td>34.8</td>
</tr>
</tbody>
</table>

Copyright 2017-2019 Standard Performance Evaluation Corporation
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPECrate2017_int_base = 33.4
SPECrate2017_int_peak = 34.8

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>12</td>
<td>670</td>
<td>28.5</td>
<td>671</td>
<td>28.5</td>
<td>667</td>
<td>28.6</td>
<td>12</td>
<td>587</td>
<td>32.5</td>
<td>584</td>
<td>32.7</td>
<td>585</td>
<td>32.7</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>12</td>
<td>531</td>
<td>32.0</td>
<td>531</td>
<td>32.0</td>
<td>532</td>
<td>31.9</td>
<td>12</td>
<td>465</td>
<td>36.5</td>
<td>465</td>
<td>36.5</td>
<td>465</td>
<td>36.5</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>12</td>
<td>504</td>
<td>38.5</td>
<td>504</td>
<td>38.5</td>
<td>504</td>
<td>38.5</td>
<td>12</td>
<td>504</td>
<td>38.5</td>
<td>504</td>
<td>38.5</td>
<td>504</td>
<td>38.5</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>12</td>
<td>666</td>
<td>23.6</td>
<td>662</td>
<td>23.8</td>
<td>665</td>
<td>23.7</td>
<td>12</td>
<td>652</td>
<td>24.1</td>
<td>651</td>
<td>24.2</td>
<td>652</td>
<td>24.2</td>
</tr>
<tr>
<td>523.xalanbmk_r</td>
<td>12</td>
<td>366</td>
<td>34.6</td>
<td>364</td>
<td>34.8</td>
<td>363</td>
<td>34.9</td>
<td>12</td>
<td>326</td>
<td>38.9</td>
<td>325</td>
<td>39.0</td>
<td>325</td>
<td>39.0</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>12</td>
<td>352</td>
<td>59.6</td>
<td>352</td>
<td>59.6</td>
<td>352</td>
<td>59.7</td>
<td>12</td>
<td>340</td>
<td>61.8</td>
<td>340</td>
<td>61.8</td>
<td>340</td>
<td>61.8</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>12</td>
<td>471</td>
<td>29.2</td>
<td>471</td>
<td>29.2</td>
<td>471</td>
<td>29.2</td>
<td>12</td>
<td>477</td>
<td>28.9</td>
<td>477</td>
<td>28.8</td>
<td>476</td>
<td>28.9</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>12</td>
<td>823</td>
<td>24.2</td>
<td>822</td>
<td>24.2</td>
<td>822</td>
<td>24.2</td>
<td>12</td>
<td>829</td>
<td>24.0</td>
<td>828</td>
<td>24.0</td>
<td>829</td>
<td>24.0</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>12</td>
<td>479</td>
<td>65.6</td>
<td>480</td>
<td>65.5</td>
<td>481</td>
<td>65.4</td>
<td>12</td>
<td>478</td>
<td>65.7</td>
<td>477</td>
<td>65.9</td>
<td>478</td>
<td>65.7</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>12</td>
<td>598</td>
<td>21.7</td>
<td>598</td>
<td>21.7</td>
<td>598</td>
<td>21.7</td>
<td>12</td>
<td>598</td>
<td>21.7</td>
<td>598</td>
<td>21.7</td>
<td>598</td>
<td>21.7</td>
</tr>
</tbody>
</table>

SPECrate2017_int_base = 33.4
SPECrate2017_int_peak = 34.8

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
    numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPECrate2017_int_base = 33.4
SPECrate2017_int_peak = 34.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

General Notes (Continued)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-fdny Thu Dec 13 08:12:21 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
  2 "physical id"s (chips)
  12 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 6
siblings : 6
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 12
On-line CPU(s) list: 0-11
Thread(s) per core: 1
Core(s) per socket: 6
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPECrate2017_int_base = 33.4
SPECrate2017_int_peak = 34.8

CPU2017 License: 9019  Test Date: Dec-2018
Test Sponsor: Cisco Systems  Hardware Availability: Aug-2017
Tested by: Cisco Systems  Software Availability: Oct-2018

Platform Notes (Continued)

Model name: Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
Stepping: 4
CPU MHz: 1655.500
CPU max MHz: 1700.0000
CPU min MHz: 800.0000
BogoMIPS: 3392.02
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 8448K
NUMA node0 CPU(s): 0-5
NUMA node1 CPU(s): 6-11
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good xtopology nonstop_tsc aperf perf_event pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb invpcid_single pni dtes64_64bitcap aesni rdrand

From /proc/cpuinfo cache data
    cache size : 8448 KB

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5
    node 0 size: 386570 MB
    node 0 free: 384374 MB
    node 1 cpus: 6 7 8 9 10 11
    node 1 size: 387054 MB
    node 1 free: 384925 MB
    node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
    MemTotal: 792192360 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

(Continued on next page)
SPEC CPU2017 Integer Rate Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPECrate2017_int_base = 33.4
SPECrate2017_int_peak = 34.8

Platform Notes (Continued)

SuSE-release:
   SUSE Linux Enterprise Server 12 (x86_64)
   VERSION = 12
   PATCHLEVEL = 2
   # This file is deprecated and will be removed in a future service pack or release.
   # Please check /etc/os-release for details about this release.

os-release:
   NAME="SLES"
   VERSION="12-SP2"
   VERSION_ID="12.2"
   PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
   ID="sles"
   ANSI_COLOR="0;32"
   CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
   Linux linux-fdny 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
   x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 13 01:46

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda2      xfs   500G  164G  337G  33% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
Memory:
   24x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2133

(End of data from sysinfo program)

Compiler Version Notes

****************************************************************************
   CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
      525.x264_r(base, peak) 557.xz_r(base, peak)
****************************************************************************

icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
*****************************************************************************

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPEC CPU2017 Integer Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPECrate2017_int_base = 33.4
SPECrate2017_int_peak = 34.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Compiler Version Notes (Continued)

CC  500.perlbench_r(peak) 502.gcc_r(peak)
------------------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
  541.leela_r(base)
------------------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
  541.leela_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
FC  548.exchange2_r(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
SPEC CPU2017 Integer Rate Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPECrate2017_int_base = 33.4
SPECrate2017_int_peak = 34.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Base Portability Flags (Continued)

502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11
502.gcc_r: icc -m32 -std=c11 -L/opt/intel/lib/ia32

C++ benchmarks (except as noted below):
icpc -m64
523.xalancbmk_r: icpc -m32 -L/opt/intel/lib/ia32

Fortran benchmarks:
ifort -m64
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

**SPEC CPU2017 Integer Rate Result**

**SPECrate2017_int_base** = 33.4

**SPECrate2017_int_peak** = 34.8

---

**Peak Portability Flags**

- 500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
- 502.gcc_r: -D_FILE_OFFSET_BITS=64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64

**Peak Optimization Flags**

**C benchmarks:**

- 500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -fno-strict-overflow -L/home/cpu2017/je5.0.1-64/
  -ljemalloc

- 502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -L/home/cpu2017/je5.0.1-32/
  -ljemalloc

- 505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -L/home/cpu2017/je5.0.1-64/
  -ljemalloc

- 525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -fno-alias
  -L/home/cpu2017/je5.0.1-64/
  -ljemalloc

- 557.xz_r: Same as 505.mcf_r

**C++ benchmarks:**

- 520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -L/home/cpu2017/je5.0.1-64/
  -ljemalloc

- 523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -L/home/cpu2017/je5.0.1-32/
  -ljemalloc

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPECrate2017_int_base = 33.4
SPECrate2017_int_peak = 34.8

Peak Optimization Flags (Continued)

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2018-12-13 11:12:20-0500.
Originally published on 2019-01-29.