## SPEC® CPU2017 Integer Rate Result

### Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5115 2.40 GHz)

<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>Tested by</th>
<th>CPU2017 License</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
</table>

- **Test Date:** Dec-2018
- **Software Availability:** Oct-2018

### SPECrate2017_int_base = 101
**SPECrate2017_int_peak = 110**

### Hardware
- **CPU Name:** Intel Xeon Gold 5115
- **Max MHz.:** 3200
- **Nominal:** 2400
- **Enabled:** 20 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 13.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Storage:** 1 x 400 GB SAS SSD
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.1 released Oct-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1

### Performance Results

<table>
<thead>
<tr>
<th>SPECrate2017_int_base = 101</th>
<th>SPECrate2017_int_peak = 110</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cores</strong></td>
<td><strong>Time (s)</strong></td>
</tr>
<tr>
<td>40</td>
<td>perlbench_r</td>
</tr>
<tr>
<td>40</td>
<td>gcc_r</td>
</tr>
<tr>
<td>40</td>
<td>mcf_r</td>
</tr>
<tr>
<td>40</td>
<td>omnetpp_r</td>
</tr>
<tr>
<td>40</td>
<td>xalancbmk_r</td>
</tr>
<tr>
<td>40</td>
<td>x264_r</td>
</tr>
<tr>
<td>40</td>
<td>deepsjeng_r</td>
</tr>
<tr>
<td>40</td>
<td>leela_r</td>
</tr>
<tr>
<td>40</td>
<td>exchange2_r</td>
</tr>
<tr>
<td>40</td>
<td>xz_r</td>
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</table>
Cisco Systems  
Cisco UCS C240 M5 (Intel Xeon Gold 5115 2.40 GHz)  

SPECrate2017_int_base = 101  
SPECrate2017_int_peak = 110

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>500.perlbench_r</td>
<td>40</td>
<td>790</td>
<td>80.6</td>
<td>789</td>
<td>80.7</td>
<td>778</td>
<td>81.9</td>
<td>40</td>
<td>652</td>
<td>97.6</td>
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<td>98.2</td>
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<td>502.gcc_r</td>
<td>40</td>
<td>674</td>
<td>84.0</td>
<td>676</td>
<td>83.8</td>
<td>647</td>
<td>87.6</td>
<td>40</td>
<td>542</td>
<td>104</td>
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<td>105</td>
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<td>505.mcf_r</td>
<td>40</td>
<td>541</td>
<td>120</td>
<td>538</td>
<td>120</td>
<td>507</td>
<td>127</td>
<td>40</td>
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<td>531</td>
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<td>520.omnetpp_r</td>
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<td>523.xalancbmk_r</td>
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<td>525.x264_r</td>
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<tr>
<td>531.deepsjeng_r</td>
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<td>94.1</td>
<td>486</td>
<td>94.2</td>
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<td>94.1</td>
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<td>541.leela_r</td>
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<td>772</td>
<td>85.8</td>
<td>755</td>
<td>87.7</td>
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<td>755</td>
<td>87.8</td>
<td>768</td>
<td>86.2</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>40</td>
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<td>197</td>
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<td>198</td>
<td>530</td>
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<td>40</td>
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<td>198</td>
<td>529</td>
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<tr>
<td>557.xz_r</td>
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<td>584</td>
<td>74.0</td>
<td>584</td>
<td>74.0</td>
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<td>40</td>
<td>576</td>
<td>74.9</td>
<td>584</td>
<td>74.0</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32":"/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>
/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
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**Cisco Systems**
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<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Dec-2018</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
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</table>

**SPECrate2017_int_base = 101**
**SPECrate2017_int_peak = 110**

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**General Notes (Continued)**

jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  

---

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Enabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f  
running on linux-klde Tue Dec 11 23:48:01 2018

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
  physical 1: cores 0 1 2 3 4 8 9 10 11 12
```

From lscpu:
```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz
```

(Continued on next page)
## Platform Notes (Continued)

- Stepping: 4
- CPU MHz: 2088.070
- CPU max MHz: 3200.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 4788.74
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 14080K
- NUMA node0 CPU(s): 0-9,20-29
- NUMA node1 CPU(s): 10-19,30-39
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu nti pнии pmlns ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm ablm abm 3dnowprefetch ida arat epb invpcid_single pln pts dtherm hwp act-window hwp-epp hwp_pkg_req intel_pt rsb_cxsw spec_ctrl stibp retopolie kaiser tpr_shadow vmmi flexpriority ept vpid fsbasebase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occu_pal

/proc/cpuinfo

```
From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
node 0 size: 386571 MB
node 0 free: 383266 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
node 1 size: 387054 MB
node 1 free: 383952 MB
node distances:
  node  0  1
  0: 10 21
  1: 21 10
```

From /proc/meminfo

```
MemTotal: 792193112 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From /etc/*release*/ etc/*version*

```
SuSE-release:
```

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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5115 2.40 GHz)

SPECCPU2017 Integer Rate Result

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CPU2017 License: 9019
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Hardware Availability: Aug-2017

Platform Notes (Continued)

SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-klde 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Dec 11 11:18

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 212G 118G 94G 56% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
Memory:
  24x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400

Compiler Version Notes

==============================================================================
CC 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
  525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================

CC 500.perlbench_r(peak) 502.gcc_r(peak)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5115 2.40 GHz)

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Tested by: Cisco Systems

Compiler Version Notes (Continued)

icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
541.leela_r(base)

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
541.leela_r(peak)

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

FC 548.exchange2_r(base, peak)

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64

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### Cisco Systems

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### Base Portability Flags (Continued)

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>505.mcf</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>520.omnetpp</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>523.xalancbmk</td>
<td>-DSPEC_LP64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>525.x264</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>531.deepsjeng</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>541.leela</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>548.exchange2</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>557.xz</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

### Base Optimization Flags

**C benchmarks:**

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

**C++ benchmarks:**

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

**Fortran benchmarks:**

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

### Peak Compiler Invocation

**C benchmarks (except as noted below):**

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/opt/intel/lib/ia32
```

**C++ benchmarks (except as noted below):**

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/opt/intel/lib/ia32
```

**Fortran benchmarks:**

```
ifort -m64
```
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Software Availability: Oct-2018

### Peak Portability Flags

- **500.perlbench_r**: -DSPEC_LP64 -DSPEC_LINUX_X64
- **502.gcc_r**: -D_FILE_OFFSET_BITS=64
- **505.mcf_r**: -DSPEC_LP64
- **520.omnetpp_r**: -DSPEC_LP64
- **523.xalancbmk_r**: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
- **525.x264_r**: -DSPEC_LP64
- **531.deepsjeng_r**: -DSPEC_LP64
- **541.leela_r**: -DSPEC_LP64
- **548.exchange2_r**: -DSPEC_LP64
- **557.xz_r**: -DSPEC_LP64

### Peak Optimization Flags

**C benchmarks:**

- **500.perlbench_r**: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -fno-strict-overflow -L/home/cpu2017/je5.0.1-64/
  -ljemalloc

- **502.gcc_r**: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -L/home/cpu2017/je5.0.1-32/ -ljemalloc

- **505.mcf_r**: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/
  -ljemalloc

- **525.x264_r**: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=3 -fno-alias
  -L/home/cpu2017/je5.0.1-64/ -ljemalloc

- **557.xz_r**: Same as 505.mcf_r

**C++ benchmarks:**

- **520.omnetpp_r**: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -L/home/cpu2017/je5.0.1-64/ -ljemalloc

- **523.xalancbmk_r**: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
  -L/home/cpu2017/je5.0.1-32/ -ljemalloc

(Continued on next page)
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SPECrate2017_int_base = 101
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Peak Optimization Flags (Continued)

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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