## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6128, 3.40 GHz)

### SPEC CPU®2017 Integer Speed Result

<table>
<thead>
<tr>
<th>Test Sponsor:</th>
<th>Cisco Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License:</td>
<td>9019</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Jan-2019</td>
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<td>Aug-2017</td>
</tr>
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<td>Software Availability:</td>
<td>Oct-2018</td>
</tr>
</tbody>
</table>

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **Compiler:** C/C++: Version 19.0.0.117 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.0.117 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.1.3e released Jun-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --

### Hardware

- **CPU Name:** Intel Xeon Gold 6128
- **Max MHz:** 3700
- **Nominal:** 3400
- **Enabled:** 24 cores, 4 chips
- **Orderable:** 2.4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 19.25 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 1 TB HDD, 7.2K RPM
- **Other:** None

### SPECspeed®2017_int_base = 8.81

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_int_base (8.81)</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s 24</td>
<td>7.46</td>
</tr>
<tr>
<td>602.gcc_s 24</td>
<td>7.27</td>
</tr>
<tr>
<td>605.mcf_s 24</td>
<td>8.27</td>
</tr>
<tr>
<td>620.omnetpp_s 24</td>
<td>5.49</td>
</tr>
<tr>
<td>623.xalancbmk_s 24</td>
<td>9.45</td>
</tr>
<tr>
<td>625.x264_s 24</td>
<td>9.09</td>
</tr>
<tr>
<td>631.deepsjeng_s 24</td>
<td>5.17</td>
</tr>
<tr>
<td>641.leela_s 24</td>
<td>4.51</td>
</tr>
<tr>
<td>648.exchange2_s 24</td>
<td>13.5</td>
</tr>
<tr>
<td>657.xz_s 24</td>
<td>21.3</td>
</tr>
</tbody>
</table>

### SPECspeed®2017_int_peak = 9.07

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<tr>
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<th>SPECspeed®2017_int_peak (9.07)</th>
</tr>
</thead>
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<tr>
<td>600.perlbench_s 24</td>
<td>9.07</td>
</tr>
<tr>
<td>602.gcc_s 24</td>
<td>9.27</td>
</tr>
<tr>
<td>605.mcf_s 24</td>
<td>11.0</td>
</tr>
<tr>
<td>620.omnetpp_s 24</td>
<td>9.09</td>
</tr>
<tr>
<td>623.xalancbmk_s 24</td>
<td>10.2</td>
</tr>
<tr>
<td>625.x264_s 24</td>
<td>6.24</td>
</tr>
<tr>
<td>631.deepsjeng_s 24</td>
<td>5.17</td>
</tr>
<tr>
<td>641.leela_s 24</td>
<td>4.51</td>
</tr>
<tr>
<td>648.exchange2_s 24</td>
<td>13.0</td>
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<td>21.6</td>
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**Tested by:** Cisco Systems  
**Test Date:** Jan-2019  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018  

### Results Table

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<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>24</td>
<td>288</td>
<td>6.17</td>
<td>282</td>
<td>6.29</td>
<td>284</td>
<td>6.24</td>
<td>24</td>
<td>238</td>
<td>7.46</td>
<td>237</td>
<td>7.50</td>
<td>238</td>
<td>7.45</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>24</td>
<td>431</td>
<td>11.0</td>
<td>431</td>
<td>11.0</td>
<td>435</td>
<td>10.9</td>
<td>24</td>
<td>429</td>
<td>11.0</td>
<td>425</td>
<td>11.1</td>
<td>425</td>
<td>11.1</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>24</td>
<td>297</td>
<td>5.49</td>
<td>295</td>
<td>5.52</td>
<td>310</td>
<td>5.26</td>
<td>24</td>
<td>287</td>
<td>5.69</td>
<td>298</td>
<td>5.47</td>
<td>292</td>
<td>5.59</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>24</td>
<td>149</td>
<td>9.54</td>
<td>150</td>
<td>9.44</td>
<td>150</td>
<td>9.45</td>
<td>24</td>
<td>138</td>
<td>10.2</td>
<td>139</td>
<td>10.2</td>
<td>138</td>
<td>10.2</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>24</td>
<td>136</td>
<td>13.0</td>
<td>135</td>
<td>13.0</td>
<td>136</td>
<td>13.0</td>
<td>24</td>
<td>136</td>
<td>13.0</td>
<td>135</td>
<td>13.0</td>
<td>136</td>
<td>13.0</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>24</td>
<td>277</td>
<td>5.17</td>
<td>277</td>
<td>5.17</td>
<td>276</td>
<td>5.18</td>
<td>24</td>
<td>281</td>
<td>5.09</td>
<td>282</td>
<td>5.09</td>
<td>281</td>
<td>5.10</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>24</td>
<td>378</td>
<td>4.51</td>
<td>378</td>
<td>4.51</td>
<td>378</td>
<td>4.51</td>
<td>24</td>
<td>382</td>
<td>4.47</td>
<td>381</td>
<td>4.48</td>
<td>381</td>
<td>4.47</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>24</td>
<td>218</td>
<td>13.5</td>
<td>218</td>
<td>13.5</td>
<td>218</td>
<td>13.5</td>
<td>24</td>
<td>218</td>
<td>13.5</td>
<td>218</td>
<td>13.5</td>
<td>218</td>
<td>13.5</td>
</tr>
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<td>24</td>
<td>290</td>
<td>21.3</td>
<td>291</td>
<td>21.2</td>
<td>287</td>
<td>21.5</td>
<td>24</td>
<td>287</td>
<td>21.6</td>
<td>286</td>
<td>21.6</td>
<td>283</td>
<td>21.8</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_int_base =** 8.81  
**SPECspeed®2017_int_peak =** 9.07

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.  

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:  
KMP_AFFINITY = "granularity=fine,scatter"  
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"  
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
`sync; echo 3 > /proc/sys/vm/drop_caches`

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

- **BIOS Settings:**
  - Intel HyperThreading Technology set to Disabled
  - CPU performance set to Enterprise
  - Power Performance Tuning set to OS Controls
  - SNC set to Disabled
  - Patrol Scrub set to Disabled

- **Sysinfo program:**
  - `/home/cpu2017/bin/sysinfo`
  - Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b091c0f
  - Running on Linux-e8np Wed Jan 30 01:31:03 2019

- **SUT (System Under Test) info as seen by some common utilities.**
  - For more information on this section, see
  - [https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

- **From `/proc/cpuinfo`**
  - model name: Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
  - 4 "physical id"s (chips)
  - 24 "processors"
  - cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from `/proc/cpuinfo` might not be reliable. Use with caution.)
    - cpu cores: 6
    - siblings: 6
    - physical 0: cores 0 6 9 10 11 13
    - physical 1: cores 0 6 9 10 11 13
    - physical 2: cores 0 3 4 9 12 14
    - physical 3: cores 0 6 9 10 11 13

- **From `lscpu`**
  - Architecture: x86_64
  - CPU op-mode(s): 32-bit, 64-bit
  - Byte Order: Little Endian
  - CPU(s): 24
  - On-line CPU(s) list: 0-23
  - Thread(s) per core: 1
  - Core(s) per socket: 6
  - Socket(s): 4
  - NUMA node(s): 4
  - Vendor ID: GenuineIntel
  - CPU family: 65
  - Model: 85
  - Model name: Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
  - Stepping: 4
  - CPU MHz: 1219.043
  - CPU max MHz: 3700.0000
  - CPU min MHz: 1200.0000
  - BogoMIPS: 6792.69
  - Virtualization: VT-x

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**SPECspeed®2017_int_base = 8.81**

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**Platform Notes (Continued)**

L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 19712K
NUMA node0 CPU(s): 0-5
NUMA node1 CPU(s): 6-11
NUMA node2 CPU(s): 12-17
NUMA node3 CPU(s): 18-23

Flags: fpu vme de pse tsc msr pae mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good ntopology nonstop_tsc
aperfmonperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpsr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avxf16c rdrand lahf_lm abm 3dnowprefetch ida arat epbiinvpcid_single pln pts
dtherm hwlpact_window hpwpkpgreq intel_pt rsb_ctxsw spec_ctrl stibp
repotline kaiser tpr_shadow vmmi flexpriority ept vpid fsqmbase tsc_adjust bni hle
avx2 smep bni2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap cliflushopt
c1wb avx512cd avx512bw avx512vl xsaveopt xsaved xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data

    cache size : 19712 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

    available: 4 nodes (0-3)
    node 0 cpus: 0 1 2 3 4 5
    node 0 size: 385624 MB
    node 0 free: 385393 MB
    node 1 cpus: 6 7 8 9 10 11
    node 1 size: 387057 MB
    node 1 free: 386762 MB
    node 2 cpus: 12 13 14 15 16 17
    node 2 size: 387057 MB
    node 2 free: 386856 MB
    node 3 cpus: 18 19 20 21 22 23
    node 3 size: 387054 MB
    node 3 free: 386836 MB

node distances:

    node 0 1 2 3
    0: 10 21 21 21
    1: 21 10 21 21
    2: 21 21 10 21
    3: 21 21 21 10

From /proc/meminfo

    MemTotal: 1583916020 kB
    HugePages_Total: 0

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Cisco Systems
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Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="$12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
uname -a:
Linux linux-e8np 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Jan 30 01:30

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 894G 122G 773G 14% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018
Memory:
48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C   | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak) |
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804

(Continued on next page)
Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6128, 3.40 GHz)

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Copyright 2017-2020 Standard Performance Evaluation Corporation

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Compiler Version Notes (Continued)

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================
C++ | 623.xalancbmk_s (peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================
C++ | 620.omnetpp_s (base, peak) 623.xalancbmk_s (base)
| 631.deepsjeng_s (base, peak) 641.leela_s (base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================
C++ | 623.xalancbmk_s (peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.0.117 Build 20180804
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==============================================================================
C++ | 620.omnetpp_s (base, peak) 623.xalancbmk_s (base)
| 631.deepsjeng_s (base, peak) 641.leela_s (base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 648.exchange2_s (base, peak)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
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**Base Compiler Invocation**

- C benchmarks: `icc -m64 -std=c11`
- C++ benchmarks: `icpc -m64`
- Fortran benchmarks: `ifort -m64`

**Base Portability Flags**

- C++ benchmarks: `-Wl,-z,muldefs -lx86_64 -Gcore-avx512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc`

**Base Optimization Flags**

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### Peak Compiler Invocation

**C benchmarks:**

```bash
icc -m64 -std=c11
```

**C++ benchmarks (except as noted below):**

```bash
icpc -m64
```

623.xalancbmk_s: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.0.117/linux/compiler/lib/ia32_lin

### Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
602.gcc_s: -DSPEC_LP64  
605.mcf_s: -DSPEC_LP64  
620.omnetpp_s: -DSPEC_LP64  
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
625.x264_s: -DSPEC_LP64  
631.deepsjeng_s: -DSPEC_LP64  
641.leela_s: -DSPEC_LP64  
648.exchange2_s: -DSPEC_LP64  
657.xz_s: -DSPEC_LP64

### Peak Optimization Flags

**C benchmarks:**

```bash
600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -fno-strict-overflow  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

```bash
602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc
```

```bash
605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
```

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Peak Optimization Flags (Continued)

605.mcf_s (continued):
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass1) -prof-use(pass2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

623.xalancbmk_s: -Wl,-z,muldefs -prof-gen(pass1) -prof-use(pass2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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