**Cisco Systems**
Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>CPU2017 License: 9019</th>
<th>Test Date: Jan-2019</th>
<th>Hardware Availability: Aug-2017</th>
<th>Software Availability: Nov-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software</td>
<td>Cisco Systems</td>
<td>Cisco Systems</td>
<td>Cisco Systems</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Threads</td>
<td>SPECspeed2017_fp_base = 134</td>
<td>SPECspeed2017_fp_peak = Not Run</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Hardware**

<table>
<thead>
<tr>
<th>CPU Name: Intel Xeon Platinum 8170</th>
<th>Max MHz.: 3700</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal: 2100</td>
<td>Enabled: 52 cores, 2 chips</td>
</tr>
<tr>
<td>Orderable: 1.2 Chips</td>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td></td>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td></td>
<td>L3: 35.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)</td>
<td>Other: None</td>
</tr>
<tr>
<td>Storage: 1 x 400 GB SAS SSD</td>
<td>Other: None</td>
</tr>
</tbody>
</table>

**Software**

<table>
<thead>
<tr>
<th>OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)</th>
<th>Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler: Version 19.0.1.144 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux</td>
<td>Parallel: Yes</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Peak Pointers: Not Applicable</td>
<td>Other: None</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPEC CPU2017 Floating Point Speed Result

SPECspeed2017_fp_base = 134
SPECspeed2017_fp_peak = Not Run

Test Date: Jan-2019
Hardware Availability: Aug-2017
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>52</td>
<td>121</td>
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<td>121</td>
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<td>490</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>52</td>
<td>101</td>
<td>165</td>
<td>101</td>
<td>165</td>
<td>165</td>
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<tr>
<td>619.lbm_s</td>
<td>52</td>
<td>54.5</td>
<td>96.2</td>
<td>54.5</td>
<td>96.1</td>
<td>96.2</td>
<td>95.8</td>
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<td>621.wrf_s</td>
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<tr>
<td>627.cam4_s</td>
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<td>106</td>
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<tr>
<td>628.pop2_s</td>
<td>52</td>
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<td>55.0</td>
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<tr>
<td>638.imagick_s</td>
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<td>143</td>
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<td>109</td>
<td>133</td>
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<tr>
<td>644.nab_s</td>
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<td>68.6</td>
<td>255</td>
<td>68.5</td>
<td>255</td>
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<tr>
<td>649.fotonik3d_s</td>
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<td>113</td>
<td>80.5</td>
<td>111</td>
<td>82.4</td>
<td>115</td>
<td>79.5</td>
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<tr>
<td>654.roms_s</td>
<td>52</td>
<td>113</td>
<td>139</td>
<td>115</td>
<td>137</td>
<td>114</td>
<td>138</td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPECspeed2017_fp_base = 134
SPECspeed2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)

SPEC CPU2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

SPEC speed2017_fp_base = 134
SPEC speed2017_fp_peak = Not Run

Cisco Systems

Test Date: Jan-2019
Hardware Availability: Aug-2017
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-klde Sat Jan 26 21:22:58 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8170 CPU @ 2.10GHz
  2 "physical id"s (chips)
  52 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
eixcerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 26
siblings : 26
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 52
On-line CPU(s) list: 0-51
Thread(s) per core: 1
Core(s) per socket: 26
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8170 CPU @ 2.10GHz
Stepping: 4
CPU MHz: 2314.226
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4190.17
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)

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</tbody>
</table>

Platform Notes (Continued)

L3 cache: 36608K
NUMA node0 CPU(s): 0-25
NUMA node1 CPU(s): 26-51
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xptr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb INVPCID_SINGLE pln pts
dtherm hwp act_window hwp_epp hwp_kgd req intel_pt rsb_cxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occosp_llc

/proc/cpuinfo cache data
cache size: 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
node 0 size: 385627 MB
node 0 free: 382779 MB
node 1 cpus: 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
51
node 1 size: 387054 MB
node 1 free: 381907 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 791226412 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

os-release:
NAME="SLES"
VERSION="12-SP2"

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)

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SPECspeed2017_fp_base = 134
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Platform Notes (Continued)

VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-klde 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 26 16:26

SPEC is set to: /home/cpu2017

Filesystem    Type  Size  Used Avail Use% Mounted on
/dev/sda3      xfs   212G  120G   92G  57% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
Memory:
    24x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes
==============================================================================
CC  619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
==============================================================================
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
FC  607.cactuBSSN_s(base)
==============================================================================
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
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Compiler Version Notes (Continued)

==============================================================================
FC  603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
------------------------------------------------------------------------------
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
CC  621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
------------------------------------------------------------------------------
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Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
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**Test Sponsor:** Cisco Systems  
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### Base Optimization Flags

**C benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

**Fortran benchmarks:**
- -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
- -nstandard-realloc-lhs -align array32byte

**Benchmarks using both Fortran and C:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
- -nstandard-realloc-lhs -align array32byte

**Benchmarks using Fortran, C, and C++:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
- -nstandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2019-01-26 10:52:57-0500.  
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