Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132, 2.60 GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed\textsuperscript{2017_int_base} = 8.85</th>
<th>SPECspeed\textsuperscript{2017_int_peak} = 9.10</th>
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<tbody>
<tr>
<td>600.perlbench_s 56</td>
<td>6.25</td>
<td>9.11</td>
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<tr>
<td>602.gcc_s 56</td>
<td>7.44</td>
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<td>605.mcf_s 56</td>
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<td>620.omnetpp_s 56</td>
<td>5.37</td>
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</tr>
<tr>
<td>623.xalancbmk_s 56</td>
<td>9.45</td>
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<tr>
<td>625.x264_s 56</td>
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<td>13.0</td>
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<td>631.deepsjeng_s 56</td>
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<td>641.leela_s 56</td>
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<td>648.exchange2_s 56</td>
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<td>13.5</td>
</tr>
<tr>
<td>657.xz_s 56</td>
<td>22.8</td>
<td>23.1</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6132
- **Max MHz:** 3700
- **Nominal:** 2600
- **Enabled:** 56 cores, 4 chips
- **Orderable:** 2.4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 19.25 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 1 TB HDD, 7.2K RPM
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
- **Compiler:** C/C++: Version 19.0.0.117 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.0.117 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.1.3e released Jun-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --
## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6132, 2.60 GHz)

**CPU2017 License:** 9019  
**Test Date:** Feb-2019  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Aug-2017  
**Tested by:** Cisco Systems  
**Software Availability:** Oct-2018

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>5.18</td>
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<td>5.10</td>
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<td>22.8</td>
<td>56</td>
<td>267</td>
<td>23.1</td>
<td>268</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_int_base = 8.85**  
**SPECspeed®2017_int_peak = 9.10**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
- `KMP_AFFINITY = "granularity=fine,scatter"`
- `LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"`
- `OMP_STACKSIZE = "192M"`

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132, 2.60 GHz)

SPEC CPU®2017 Integer Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_int_base = 8.85
SPECspeed®2017_int_peak = 9.10

Test Date: Feb-2019
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bce091c0f
running on linux-e8np Mon Feb 18 20:37:15 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6132 CPU @ 2.60GHz
 4 "physical id"s (chips)
56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 14
siblings : 14
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 56
On-line CPU(s) list: 0-55
Thread(s) per core: 1
Core(s) per socket: 14
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6132 CPU @ 2.60GHz
Stepping: 4
CPU MHz: 1800.701
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 5194.43
Virtualization: VT-x

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132, 2.60 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_int_base = 8.85
SPECspeed®2017_int_peak = 9.10

Platform Notes (Continued)

L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 19712K
NUMA node0 CPU(s): 0-13
NUMA node1 CPU(s): 14-27
NUMA node2 CPU(s): 28-41
NUMA node3 CPU(s): 42-55

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnumm flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 rome invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsavesopt xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13
node 0 size: 385623 MB
node 0 free: 385407 MB
node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27
node 1 size: 387057 MB
node 1 free: 386777 MB
node 2 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41
node 2 size: 387057 MB
node 2 free: 386794 MB
node 3 cpus: 42 43 44 45 46 47 48 49 50 51 52 53 54 55
node 3 size: 387054 MB
node 3 free: 386727 MB
node distances:

node 0 1 2 3
0: 10 21 21 21
1: 21 10 10 21
2: 21 21 10 21
3: 21 21 21 10

From /proc/meminfo
MemTotal: 1583915624 kB
HugePages_Total: 0

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132, 2.60 GHz)

<table>
<thead>
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</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

```
Hugepagesize:  2048 kB
From /etc/*release* /etc/*version*
SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-e8np 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
    x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Feb 18 20:34
SPEC is set to: /home/cpu2017
```

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda1      xfs   894G  166G  729G  19% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018
Memory:
    48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

```c
600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132, 2.60 GHz)

CPUs: 10x Intel(R) Xeon(R) Gold 6132 (2.60 GHz)

SPECspeed®2017_int_base = 8.85
SPECspeed®2017_int_peak = 9.10

Test Sponsor: Cisco Systems
Test Date: Feb-2019
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Compiler Version Notes (Continued)

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++ | 623.xalancbmk_s(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++ | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base)
    | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++ | 623.xalancbmk_s(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++ | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base)
    | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
Fortran | 648.exchange2_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
**SPEC CPU®2017 Integer Speed Result**

**Cisco Systems**
Cisco UCS C480 M5 (Intel Xeon Gold 6132, 2.60 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
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<td>Test Sponsor: Cisco Systems</td>
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</tr>
</tbody>
</table>

**SPECspeed®2017_int_base = 8.85**

| SPECspeed®2017_int_peak = 9.10 |

---

### Base Compiler Invocation

C benchmarks:
```bash
c -m64 -std=c11
```

C++ benchmarks:
```bash
icpc -m64
```

Fortran benchmarks:
```bash
ifort -m64
```

---

### Base Portability Flags

- 600.perlbench_s: `–DSPEC_LP64 –DSPEC_LINUX_X64`
- 602.gcc_s: `–DSPEC_LP64`
- 605.mcf_s: `–DSPEC_LP64`
- 620.omnetpp_s: `–DSPEC_LP64`
- 623.xalancbmk_s: `–DSPEC_LP64 –DSPEC_LINUX`
- 625.x264_s: `–DSPEC_LP64`
- 631.deepsjeng_s: `–DSPEC_LP64`
- 641.leela_s: `–DSPEC_LP64`
- 648.exchange2_s: `–DSPEC_LP64`
- 657.xz_s: `–DSPEC_LP64`

---

### Base Optimization Flags

**C benchmarks:**
```bash
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

**C++ benchmarks:**
```bash
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc
```

**Fortran benchmarks:**
```bash
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc
```
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132, 2.60 GHz)

| SPEC®2017_int_base = 8.85 |
| SPEC®2017_int_peak = 9.10 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Feb-2019
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Peak Compiler Invocation

C benchmarks:
```bash
c -m64 -std=c11
```

C++ benchmarks (except as noted below):
```bash
icpc -m64
```

623.xalancbmk_s: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.0.117/linux/compiler/lib/ia32_lin

Fortran benchmarks:
```bash
ifort -m64
```

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
```bash
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP

(Continued on next page)
## SPEC CPU®2017 Integer Speed Result

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132, 2.60 GHz)

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### SPECspeed®2017 Int Base = 8.85

### SPECspeed®2017 Int Peak = 9.10

---

## Peak Optimization Flags (Continued)

605.mcf_s (continued):
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

625.x264_s:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -gopenmp -DSPEC_OPENMP`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

657.xz_s: Same as 602.gcc_s

### C++ benchmarks:

620.omnetpp_s:
- `-Wl,-z,muldefs -prof-gen(pass1) -prof-use(pass2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

623.xalancbmk_s:
- `-Wl,-z,muldefs -prof-gen(pass1) -prof-use(pass2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

### Fortran benchmarks:

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

---

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-02-18 20:37:14-0500.
Report generated on 2020-07-01 14:47:30 by CPU2017 PDF formatter v6255.
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