Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8280, 2.70GHz)

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Mar-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** Nov-2018

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate2017_fp_base</th>
<th>SPECrate2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>56</td>
<td>Not Run</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>56</td>
<td>129</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>56</td>
<td>134</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>56</td>
<td>68.1</td>
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<td>519.lbm_r</td>
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<td>527.cam4_r</td>
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<tr>
<td>538.imagick_r</td>
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<td>544.nab_r</td>
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<tr>
<td>554.roms_r</td>
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**Software**

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</th>
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<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux</td>
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<tr>
<td>Parallel:</td>
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<td>Firmware:</td>
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<tr>
<td>File System:</td>
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**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** Not Applicable  
**Other:** None

---

**Hardware**

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon Platinum 8280</th>
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<tbody>
<tr>
<td>Max MHz.:</td>
<td>4000</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2700</td>
</tr>
<tr>
<td>Enabled:</td>
<td>28 cores, 1 chip, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1.2 Chips</td>
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<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
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<td>L3:</td>
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<tr>
<td>Memory:</td>
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<tr>
<td>Storage:</td>
<td>1 x 1.9 TB SSD SAS</td>
</tr>
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<td>Other:</td>
<td>None</td>
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</tbody>
</table>
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8280, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

SPECrate2017_fp_base = 141
SPECrate2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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</tr>
</tbody>
</table>

SPECrate2017_fp_base = 141
SPECrate2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8280, 2.70GHz)

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SPECrate2017_fp_base = 141
SPECrate2017_fp_peak = Not Run

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-acp5 Thu Mar 14 15:25:17 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8280 CPU @ 2.70GHz
  1  "physical id"s (chips)
    56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 56
On-line CPU(s) list: 0-55
Thread(s) per core: 2
Core(s) per socket: 28
Socket(s): 1
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85

(Continued on next page)
Platform Notes (Continued)

Model name: Intel(R) Xeon(R) Platinum 8280 CPU @ 2.70GHz
Stepping: 7
CPU MHz: 2700.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 39424K
NUMA node0 CPU(s): 0-3,7-9,14-17,21-23,28-31,35-37,42-45,49-51
NUMA node1 CPU(s): 4-6,10-13,18-20,24-27,32-34,38-41,46-48,52-55
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
         pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb
         rdtsdp rdts魄 bts rep_good nopl xtopology
         nonstop_tsc cpuid tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid_single
         mtrte mpt mvpt mvtste mvtts ept pmls aes xsave avx f16c rdrand
         rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
         xsaveopt xsavec xsaves cqm_11c cqm_occup_line cqm_mbm_total
         cqm_mbm_local ibpb ibrs stibp
dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospk
         avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 39424 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 7 8 9 14 15 16 17 21 22 23 28 29 30 31 35 36 37 42 43 44 45 49 50
    node 0 size: 192066 MB
    node 0 free: 183607 MB
    node 1 cpus: 4 5 6 10 11 12 13 18 19 20 24 25 26 27 32 33 34 38 39 40 41 46 47 48 52 53
    node 1 size: 193518 MB
    node 1 free: 187062 MB
    node distances:
      node 0 1
      0: 10 11
      1: 11 10

From /proc/meminfo
  MemTotal: 394839472 KB

(Continued on next page)
Platform Notes (Continued)

HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
    os-release:
        NAME="SLES"
        VERSION="15"
        VERSION_ID="15"
        PRETTY_NAME="SUSE Linux Enterprise Server 15"
        ID="sles"
        ID_LIKE="suse"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-acp5 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown):        Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Mar 14 11:05

SPEC is set to: /home/cpu2017
    Filesystem      Type Size Used Avail Use% Mounted on
    /dev/sdb1      xfs  1.9T  70G  1.8T  4% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

    BIOS Cisco Systems, Inc. C240M5.4.0.3.34.0301190218 03/01/2019
    Memory:
        12x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
        12x NO DIMM NO DIMM

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8280, 2.70GHz)

Spec CPU2017 Floating Point Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECraten2017_fp_base = 141
SPECraten2017_fp_peek = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

---------------------------------------------------------------------
CXXC 508.namd_r(base) 510.parest_r(base)
---------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

---------------------------------------------------------------------
CC 511.povray_r(base) 526.blender_r(base)
---------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

---------------------------------------------------------------------
FC 507.cactuBSSN_r(base)
---------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

---------------------------------------------------------------------
FC 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
---------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
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</tr>
</tbody>
</table>

### Compiler Version Notes (Continued)

```
CC  521.wrf_r(base) 527.cam4_r(base)
```

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

### Base Compiler Invocation

**C benchmarks:**
icc -m64 -std=c11

**C++ benchmarks:**
icpc -m64

**Fortran benchmarks:**
ifort -m64

**Benchmarks using both Fortran and C:**
ifort -m64 icc -m64 -std=c11

**Benchmarks using both C and C++:**
icpc -m64 icc -m64 -std=c11

**Benchmarks using Fortran, C, and C++:**
icpc -m64 icc -m64 -std=c11 ifort -m64

### Base Portability Flags

503.bwaves_r: -DSPEC_LP64  
507.cactuBSSN_r: -DSPEC_LP64  
508.namd_r: -DSPEC_LP64  
510.parest_r: -DSPEC_LP64  
511.povray_r: -DSPEC_LP64  
519.ibm_r: -DSPEC_LP64  
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian  
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char  
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG  
538.imagick_r: -DSPEC_LP64

(Continued on next page)
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Base Portability Flags (Continued)
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revI.xml
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<td>Apr-2019</td>
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<td>Software Availability:</td>
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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