## Lenovo Global Technology

**ThinkSystem SR630**  
(2.10 GHz, Intel Xeon Silver 4216)

- **CPU2017 License:** 9017  
- **Test Sponsor:** Lenovo Global Technology  
- **Tested by:** Lenovo Global Technology  
- **Test Date:** Apr-2019  
- **Hardware Availability:** Apr-2019  
- **Software Availability:** Nov-2018

### SPECrate2017_int_base

- **Value:** 174

### SPECrate2017_int_peak

- **Value:** Not Run

### Hardware

- **CPU Name:** Intel Xeon Silver 4216  
- **Max MHz.:** 3200  
- **Nominal:** 2100  
- **Enabled:** 32 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 22 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R, running at 2400)  
- **Storage:** 1 x 800 GB SATA SSD  
- **Other:** None

### Software

- **OS:** Red Hat Enterprise Linux Server release 7.6 (Maipo)  
- **Kernel:** 3.10.0-957.el7.x86_64  
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++  
  Compiler Build 20181018 for Linux;  
  Fortran: Version 19.0.1.144 of Intel Fortran  
  Compiler Build 20181018 for Linux  
- **Parallel:** No  
- **Firmware:** Lenovo BIOS Version IVE135P 2.10 released Feb-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** None

### SPECrate2017_int_base (174)**

<table>
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<th>Specrate2017_int_base</th>
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SPECrate2017_int_base = 174
SPECrate2017_int_peak = Not Run

Results Table

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<td>584</td>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017-1.0.5-ic19.0u1/lib/intel64"
Bins compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Files/system page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
**Lenovo Global Technology**

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<table>
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<tbody>
<tr>
<td>174</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

---

**CPU2017 License:** 9017

**Test Sponsor:** Lenovo Global Technology

**Tested by:** Lenovo Global Technology

---

**General Notes (Continued)**

Yes: The test sponsor attests, as of date of publication, that CVE-2018-3640 (Spectre variant 3a) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2018-3639 (Spectre variant 4) is mitigated in the system as tested and documented.

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**Platform Notes**

**BIOS configuration:**
Choose Operating Mode set to Maximum Performance
Choose Operating Mode set to Custom Mode
C-states set to Legacy
SNC set to Enable
Trusted Execution Technology set to Enable
Stale AtoS set to Enable
LLC dead line alloc set to Disable
Sysinfo program /home/cpu2017-1.0.5-ic19.0u1/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on localhost.localdomain Mon Apr 15 21:10:35 2019

**SUT (System Under Test) info as seen by some common utilities.**
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2  "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu:

```
Architecture:      x86_64
CPU op-mode(s):    32-bit, 64-bit
Byte Order:        Little Endian
CPU(s):            64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s):         2
NUMA node(s):      4
Vendor ID:         GenuineIntel
CPU family:        6
```

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*(Continued on next page)*
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| SPECrate2017_int_base = 174 |
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CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Test Date: Apr-2019
Tested by: Lenovo Global Technology
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Platform Notes (Continued)

Model: 85
Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-3,8-11,32-35,40-43
NUMA node1 CPU(s): 4-7,12-15,36-39,44-47
NUMA node2 CPU(s): 16-19,24-27,48-51,56-59
NUMA node3 CPU(s): 20-23,28-31,52-55,60-63
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch epb cat_l3 intel_pt ssbd mb aibr ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ermal invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl vsxveopt xsaveopt xsave xgetbv1 cqm_l1c cqm_occup_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pku ospke avx512_vnni spec_ctrl intel_stibp flush_l1d arch_capabilities

From /proc/cpuinfo cache data

cache size : 22528 KB

(Continued on next page)
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SPEC CPU2017 Integer Rate Result
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Software Availability: Nov-2018

Platform Notes (Continued)

1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 395878592 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*

os-release:
NAME="Red Hat Enterprise Linux Server"
VERSION="7.6 (Maipo)"
ID="rhel"
ID_LIKE="fedora"
VARIANT="Server"
VARIANT_ID="server"
VERSION_ID="7.6"
PRETTY_NAME="Red Hat Enterprise Linux Server 7.6 (Maipo)"
redhat-release: Red Hat Enterprise Linux Server release 7.6 (Maipo)
system-release: Red Hat Enterprise Linux Server release 7.6 (Maipo)

uname -a:
Linux localhost.localdomain 3.10.0-957.el7.x86_64 #1 SMP Thu Oct 4 20:48:51 UTC 2018
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: Load fences, __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS

run-level 3 Apr 15 21:09

SPEC is set to: /home/cpu2017-1.0.5-ic19.0u1

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 xfs 689G 21G 668G 4% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Lenovo -[IVE135P-2.10]- 02/13/2019
Memory:
24x Samsung M393A2K43CB2-CVF 16 GB 2 rank 2933, configured at 2400

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# SPEC CPU2017 Integer Rate Result

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</table>

**CPU2017 License:** 9017  
**Software Availability:** Nov-2018

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**Platform Notes (Continued)**

(End of data from sysinfo program)

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**Compiler Version Notes**

```
CC  500.perlibench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base)
    557.xz_r(base)
-----------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
    541.leela_r(base)
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

FC  548.exchange2_r(base)
-----------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

**Base Compiler Invocation**

- **C benchmarks:**
  - icc -m64 -std=c11

- **C++ benchmarks:**
  - icpc -m64

- **Fortran benchmarks:**
  - ifort -m64
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**SPECrate2017_int_base = 174**  
**SPECrate2017_int_peak = Not Run**

### Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

- Wl, -z, multidefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- qopt-mem-layout-trans=4  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64  
- lqkmalloc

**C++ benchmarks:**

- Wl, -z, multidefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- qopt-mem-layout-trans=4  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64  
- lqkmalloc

**Fortran benchmarks:**

- Wl, -z, multidefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64  
- lqkmalloc

The flags files that were used to format this result can be browsed at:

http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-A.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-A.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-04-15 09:10:34-0400.