Lenovo Global Technology

ThinkSystem SD530

(2.50 GHz, Intel Xeon Silver 4215)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

SPECrater2017_fp_base = 106
SPECrater2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>Software</th>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 12 SP4 (x86_64)</th>
</tr>
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<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.1.144 of Intel C/C++</td>
<td></td>
</tr>
<tr>
<td>Compiler Build:</td>
<td>20181018 for Linux</td>
<td></td>
</tr>
<tr>
<td>Fortran:</td>
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<tr>
<td>Compiler Build:</td>
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<tr>
<td>Parallel:</td>
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<tr>
<td>Firmware:</td>
<td>Lenovo BIOS Version TEE135R 2.10 released Feb-2019</td>
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<tr>
<td>File System:</td>
<td>xfs</td>
<td></td>
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<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
<td></td>
</tr>
<tr>
<td>Base Pointers:</td>
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<tr>
<td>Peak Pointers:</td>
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<tr>
<td>Other:</td>
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<table>
<thead>
<tr>
<th>Hardware</th>
<th>CPU Name:</th>
<th>Intel Xeon Silver 4215</th>
</tr>
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<tbody>
<tr>
<td>Max MHz.:</td>
<td>2500</td>
<td></td>
</tr>
<tr>
<td>Nominal:</td>
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</tr>
<tr>
<td>Enabled:</td>
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<tr>
<td>Orderable:</td>
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<tr>
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<td>L2:</td>
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<tr>
<td>L3:</td>
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<td>Memory:</td>
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<td>Storage:</td>
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<td>Other:</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<tr>
<td>508.namd_r</td>
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<td>519.lbm_r</td>
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<tr>
<td>521.wrf_r</td>
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<td>526.blender_r</td>
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</tr>
<tr>
<td>527.cam4_r</td>
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<tr>
<td>538.imagick_r</td>
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<tr>
<td>544.nab_r</td>
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<tr>
<td>549.fotonik3d_r</td>
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<td>554.roms_r</td>
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</table>

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Dec-2018
Lenovo Global Technology
ThinkSystem SD530
(2.50 GHz, Intel Xeon Silver 4215)

CPU2017 License: 9017
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Results Table

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</tr>
</tbody>
</table>

SPECrate2017_fp_base = 106
SPECrate2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017-1.0.5-ic19.0u1/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Lenovo Global Technology  
ThinkSystem SD530  
(2.50 GHz, Intel Xeon Silver 4215)  

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>SPECrate2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**General Notes (Continued)**

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2018-3640 (Spectre variant 3a) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2018-3639 (Spectre variant 4) is mitigated in the system as tested and documented.

**Platform Notes**

BIOS configuration:
Choose Operating Mode set to Maximum Performance
Choose Operating Mode set to Custom Mode
Intel Virtualization Technology set to Disable
MONITOR/MWAIT set to Enable
Sysinfo program /home/cpu2017-1.0.5-ic19.0ul/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-rofd Mon Apr 22 17:14:50 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
  2 "physical id"s (chips)
  32 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 8
    siblings : 16
    physical 0: cores 0 1 2 3 4 5 6 7
    physical 1: cores 0 1 2 3 4 5 6 7
```

From lscpu:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                32
On-line CPU(s) list:   0-31
Thread(s) per core:    2
Core(s) per socket:    8
Socket(s):             2
NUMA node(s):          2
Vendor ID:             GenuineIntel
```

(Continued on next page)
### Lenovo Global Technology

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<table>
<thead>
<tr>
<th>SPECrate2017_fp_base</th>
<th>106</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**SPEC CPU2017 Floating Point Rate Result**  
Copyright 2017-2019 Standard Performance Evaluation Corporation

---

**Platform Notes (Continued)**

```plaintext
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
Stepping:              6
CPU MHz:               2500.000
CPU max MHz:           3500.0000
CPU min MHz:           1000.0000
BogoMIPS:              5000.00
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              11264K
NUMA node0 CPU(s):     0-7,16-23
NUMA node1 CPU(s):     8-15,24-31
Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                       pat pse36 clflush dts msr pae mce cx8 ht tm pbe syscall nx pdpe1gb rdtscp
                       lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                       aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
                       xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abtm mcm候 xtico tr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
```

From `numactl --hardware`

```plaintext
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

From `/proc/cpuinfo`

```plaintext
cache size : 11264 KB
```

From `/proc/meminfo`

```plaintext
MemTotal:       197703828 kB
HugePages_Total:       0
```

(Continued on next page)
Lenovo Global Technology
ThinkSystem SD530
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SPECrates2017_fp_base = 106
SPECrates2017_fp_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 4
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.

os-release:
  NAME="SLES"
  VERSION="12-SP4"
  VERSION_ID="12.4"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP4"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp4"

uname -a:
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_PW

run-level 3 Apr 22 17:12

SPEC is set to: /home/cpu2017-1.0.5-ic19.0u1
  Filesystem          Type  Size  Used Avail Use% Mounted on
  /dev/md126p3        xfs   743G   31G  712G   5% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Lenovo -[TEE135R-2.10]- 02/26/2019
  Memory:
    4x NO DIMM NO DIMM
    12x SK Hynix HMA82GR7CJR8N-WM 16 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)
## Lenovo Global Technology

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**Test Date:**  
**Hardware Availability:** Apr-2019  
**Software Availability:** Dec-2018

### Compiler Version Notes

```plaintext
==============================================================================
CC  519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
CXXC 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
CC  511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
FC  507.cactuBSSN_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
FC  503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
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(Continued on next page)
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Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Dec-2018

Compiler Version Notes (Continued)

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CC  521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.1bm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsIGNED-char

(Continued on next page)
Lenovo Global Technology

ThinkSystem SD530
(2.50 GHz, Intel Xeon Silver 4215)

**SPEC CPU2017 Floating Point Rate Result**

**CPU2017 License:** 9017
**Test Date:** Apr-2019
**Test Sponsor:** Lenovo Global Technology
**Hardware Availability:** Apr-2019
**Tested by:** Lenovo Global Technology
**Software Availability:** Dec-2018

**SPECrate2017_fp_base =** 106
**SPECrate2017_fp_peak =** Not Run

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**Base Portability Flags (Continued)**

527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

---

**Base Optimization Flags**

**C benchmarks:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

**C++ benchmarks:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

**Fortran benchmarks:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

**Benchmarks using both Fortran and C:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

**Benchmarks using both C and C++:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

**Benchmarks using Fortran, C, and C++:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

---

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:

# Lenovo Global Technology

ThinkSystem SD530  
(2.50 GHz, Intel Xeon Silver 4215)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-04-22 05:14:49-0400.  