**SPEC® CPU2017 Floating Point Speed Result**

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
ProLiant DL380 Gen10  
(2.20 GHz, Intel Xeon Silver 4216)

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE  

<table>
<thead>
<tr>
<th>SPECspeed2017_fp_base</th>
<th>SPECspeed2017_fp_peak</th>
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<tbody>
<tr>
<td>= 102</td>
<td>= Not Run</td>
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<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Apr-2019</th>
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<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
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### Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Count</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>32</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>32</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>32</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>32</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>32</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>32</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>32</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>32</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>32</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>32</td>
</tr>
</tbody>
</table>

### Hardware

**CPU Name:** Intel Xeon Silver 4216  
**Max MHz.:** 3200  
**Nominal:** 2100  
**Enabled:** 32 cores, 2 chips  
**Orderable:** 1, 2 chip(s)  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I-D on chip per core  
**L3:** 22 MB I+D on chip per chip  
**Other:** None  
**Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)  
**Storage:** 1 x 480 GB SATA SSD, RAID 0  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 15 (x86_64)  
**Kernel:** 4.12.14-23-default  
**Compiler:** C/C++: Version 19.0.2.187 of Intel C/C++ Compiler Build 20190117 for Linux; Fortran: Version 19.0.2.187 of Intel Fortran Compiler Build 20190117 for Linux  
**Parallel:** Yes  
**Firmware:** HPE BIOS Version U30 02/02/2019 released Apr-2019  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** Not Applicable  
**Other:** None
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SPECspeed2017_fp_base = 102
SPECspeed2017_fp_peak = Not Run

Results Table

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<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
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<td>142</td>
<td>111</td>
<td>142</td>
<td>111</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=core,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9–7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling

(Continued on next page)
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Platform Notes (Continued)

Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Peak Frequency Compute
Energy/Performance Bias set to Balanced Power
Workload Profile set to Custom
Numa Group Size Optimization set to Flat
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-9mbf Tue Apr 16 19:55:54 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

  model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2  "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 16
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:

  Architecture:           x86_64
  CPU op-mode(s):         32-bit, 64-bit
  Byte Order:             Little Endian
  CPU(s):                 32
  On-line CPU(s) list:    0-31
  Thread(s) per core:     1
  Core(s) per socket:     16
  Socket(s):              2
  NUMA node(s):           2
  Vendor ID:              GenuineIntel
  CPU family:             6
  Model:                  85
  Model name:             Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  Stepping:               6
  CPU MHz:                2100.000
  BogoMIPS:               4200.00
  Virtualization:         VT-x
  L1d cache:              32K
  L1i cache:              32K

(Continued on next page)
Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 22582K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pbebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmrperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpdr pcdm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdpl_l3 invpcid_single intel_ppl intel tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mxpx rdts_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsave xgetbv xsavec cmpmfn cmpmfc cmpmft cmpmft by ibpb ibrs stibp dtherm
ida arat pln pts pkd ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size: 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  node 0 size: 193018 MB
  node 0 free: 192537 MB
  node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
  node 1 size: 193335 MB
  node 1 free: 193019 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 395626560 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"

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Platform Notes (Continued)

uname -a:
   Linux linux-9mbf 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Apr 16 19:53

SPEC is set to: /home/cpu2017
   Filesystem     Type  Size  Used Avail Use% Mounted on
   /dev/sdb4      xfs   436G  310G  127G  71% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS HPE U30 02/02/2019
   Memory:
      24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

--------------------------------------------------------------------------------------------------
CC  619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
--------------------------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------------------------

--------------------------------------------------------------------------------------------------
FC  607.cactuBSSN_s(base)
--------------------------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,

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Compiler Version Notes (Continued)

Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R)
64, Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64

(Continued on next page)
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### Base Portability Flags (Continued)

- 607.cactuBSSN_s: -DSPEC_LP64  
- 619.ibm_s: -DSPEC_LP64  
- 621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian  
- 627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG  
- 628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl  
- 638.imagick_s: -DSPEC_LP64  
- 644.nab_s: -DSPEC_LP64  
- 649.fotonik3d_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl  
- 654.roms_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-qopt-prefetch-issue-excl-hint -ansi-alias -complex-limited-range

**Fortran benchmarks:**

-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
-qopt-prefetch-issue-excl-hint -ansi-alias -complex-limited-range -nostandard-realloc-lhs

**Benchmarks using both Fortran and C:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-qopt-prefetch-issue-excl-hint -ansi-alias -complex-limited-range -nostandard-realloc-lhs

**Benchmarks using Fortran, C, and C++:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-qopt-prefetch-issue-excl-hint -ansi-alias -complex-limited-range -nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at  
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.html  
http://www.spec.org/cpu2017/flags/HPE-ic19.0ul-flags-linux64.html

You can also download the XML flags sources by saving the following links:  
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.xml  
http://www.spec.org/cpu2017/flags/HPE-ic19.0ul-flags-linux64.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-04-16 19:55:53-0400.