Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>98.5</th>
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</thead>
<tbody>
<tr>
<td>SPECrate2017_int_peak</td>
<td>Not Run</td>
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</table>

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

<table>
<thead>
<tr>
<th>CPU Name: Intel Xeon Silver 4215</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max MHz.: 3500</td>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
</tr>
<tr>
<td>Nominal: 2500</td>
<td>Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux</td>
</tr>
<tr>
<td>Enabled: 16 cores, 2 chips, 2 threads/core</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>Orderable: 1,2 chips</td>
<td>Firmware: Version 4.0.2.193 released Dec-2018</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
<td>File System: btrfs</td>
</tr>
<tr>
<td>Cache L2: 1 MB I-D on chip per core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Cache L3: 11 MB I+D on chip per chip</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Other: None</td>
<td>Peak Pointers: Not Applicable</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)</td>
<td>Other: None</td>
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<tr>
<td>Storage: 1 x 400 GB SATA SSD</td>
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Page 1 Standard Performance Evaluation Corporation (info@spec.org) https://www.spec.org/
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SPECrate2017_int_base = 98.5
SPECrate2017_int_peak = Not Run

Results Table

<table>
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<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Seconds</th>
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</tr>
</thead>
<tbody>
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<td>679</td>
<td>75.0</td>
<td>676</td>
<td>75.3</td>
<td>679</td>
<td>75.0</td>
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<tr>
<td>502.gcc_r</td>
<td>32</td>
<td>550</td>
<td>82.3</td>
<td>550</td>
<td>82.4</td>
<td>544</td>
<td>83.3</td>
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<tr>
<td>505.mcf_r</td>
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<td>137</td>
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<td>137</td>
<td>376</td>
<td>137</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
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<td>640</td>
<td>65.6</td>
<td>640</td>
<td>65.6</td>
<td>641</td>
<td>65.5</td>
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<td>280</td>
<td>121</td>
<td>282</td>
<td>120</td>
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<tr>
<td>525.x264_r</td>
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<td>531.deepsjeng_r</td>
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<td>81.4</td>
<td>451</td>
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<td>541.leela_r</td>
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<td>548.exchange2_r</td>
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<tr>
<td>557.xz_r</td>
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<td>537</td>
<td>64.3</td>
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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
  numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
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Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)  

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General Notes (Continued)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Enabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- IMC Interleaving set to Auto
- Patrol Scrub set to Disabled
- Sysinfo program /home/cpu2017/bin/sysinfo
- Rev: r5974 of 2018-05-19 9bcede8f2999c33d61f64985e45859ea9
- running on linux-jimm Sat Apr 27 22:05:10 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
- 2 "physical id"s (chips)
- 32 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores: 8
  - siblings: 16
  - physical 0: cores 0 1 2 3 4 5 6 7
  - physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 32
- On-line CPU(s) list: 0-31
- Thread(s) per core: 2
- Core(s) per socket: 8
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
- Stepping: 6
- CPU MHz: 2500.000

(Continued on next page)
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Platform Notes (Continued)

CPU max MHz: 3500.0000
CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpсрf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pdcd dca sse4_1 sse4_2 x2apic movbe popcnt
vtid fs.gsbase tsc_adjust bmi1 hle avx2 smep bmi2 invpcid rdt_a
axv512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
lbb ibrs stibp dtherm ida arat p1n pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 385637 MB
node 0 free: 385107 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 387027 MB
node 1 free: 386587 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 791209844 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:

(Continued on next page)
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Platform Notes (Continued)

NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-jimm 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Apr 27 22:01

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 btrfs 370G 6.7G 362G 2% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.4.0.2.193.1203182037 12/03/2018
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base)
557.xz_r(base)
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
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Compiler Version Notes (Continued)

==============================================================================
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
  541.leela_r(base)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
FC  548.exchange2_r(base)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64  -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64  -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
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Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revI.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-04-28 03:35:09-0400.