# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4208, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>83.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

### CPU2017 License: 9019

**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Apr-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** Nov-2018

### Hardware

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<td>63.4</td>
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</tr>
<tr>
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<td>59.0</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>104.4</td>
</tr>
<tr>
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<td>148.8</td>
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<tr>
<td>531.deepsjeng_r</td>
<td>68.3</td>
</tr>
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<td>143.4</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>56.1</td>
</tr>
</tbody>
</table>

#### CPU Name:
Intel Xeon Silver 4208

#### Max MHz:
3200

#### Nominal:
2100

#### Enabled:
16 cores, 2 chips, 2 threads/core

#### Orderable:
1.2 chips

#### Cache L1:
32 KB I + 32 KB D on chip per core

#### L2:
1 MB I+D on chip per core

#### L3:
11 MB I+D on chip per chip

#### Other:
None

#### Memory:
768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)

#### Storage:
1 x 600 GB SAS HDD, 10K RPM

#### Other:
None

### Software

#### OS:
SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default

#### Compiler:
C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux

#### Parallel:
No

#### Firmware:
Version 4.0.3.28 released Feb-2019

#### File System:
btrfs

#### System State:
Run level 3 (multi-user)

#### Base Pointers:
64-bit

#### Peak Pointers:
Not Applicable

#### Other:
None

#### Power Management:
--
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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</tr>
</thead>
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<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>799</td>
<td>63.8</td>
<td>802</td>
<td>63.5</td>
<td>801</td>
<td>63.6</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>32</td>
<td>622</td>
<td>72.9</td>
<td>624</td>
<td>72.6</td>
<td>623</td>
<td>72.8</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>32</td>
<td>443</td>
<td>117</td>
<td>440</td>
<td>118</td>
<td>440</td>
<td>118</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>32</td>
<td>711</td>
<td>59.0</td>
<td>712</td>
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</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>32</td>
<td>325</td>
<td>104</td>
<td>325</td>
<td>104</td>
<td>326</td>
<td>104</td>
</tr>
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<td>32</td>
<td>380</td>
<td>147</td>
<td>378</td>
<td>148</td>
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<td>148</td>
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<td>32</td>
<td>537</td>
<td>68.3</td>
<td>538</td>
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<td>537</td>
<td>68.3</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>32</td>
<td>853</td>
<td>62.2</td>
<td>855</td>
<td>61.9</td>
<td>841</td>
<td>63.0</td>
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<td>587</td>
<td>143</td>
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<td>143</td>
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<td>143</td>
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<td>32</td>
<td>616</td>
<td>56.1</td>
<td>616</td>
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<td>617</td>
<td>56.0</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 83.7**

**SPECrate®2017_int_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

```shell
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

Memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```shell
    sync; echo 3> /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```shell
    numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4208, 2.10GHz)

SPECrate®2017_int_base =  83.7
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

General Notes (Continued)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcede8f2999c33d61f64985e45859ea9
running on linux-3usq Sun Apr 28 01:14:11 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
 physical 0: cores 0 1 2 3 4 5 6 7
 physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000

(Continued on next page)
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Platform Notes (Continued)

CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 tpxr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
from /proc/cpuinfo cache data

cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 385634 MB
node 0 free: 385054 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 387027 MB
node 1 free: 386604 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 791206632 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
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Platform Notes (Continued)

NAME="SLES"  
VERSION="15"  
VERSION_ID="15"  
PRETTY_NAME="SUSE Linux Enterprise Server 15"  
ID="sles"  
ID_LIKE="suse"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:  
Linux linux-3usq 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)  
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected  
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW  
run-level 3 Apr 28 01:13

SPEC is set to: /home/cpu2017  
Filesystem Type Size Used Avail Use% Mounted on  
/dev/sdc1 btrfs 559G 6.8G 551G 2% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.  
BIOS Cisco Systems, Inc. C220M5.4.0.3.28.0225191830 02/25/2019  
Memory:  
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================  
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)  
| 525.x264_r(base) 557.xz_r(base)

==============================================================================  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
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### Compiler Version Notes (Continued)

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Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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<th>Fortran</th>
<th>548.exchange2_r(base)</th>
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.1.144 Build 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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### Base Compiler Invocation

C benchmarks:  
```bash  
icc -m64 -std=c11  
```

C++ benchmarks:  
```bash  
icpc -m64  
```

Fortran benchmarks:  
```bash  
ifort -m64  
```

### Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64
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**SPECrate®2017_int_base** = 83.7
**SPECrate®2017_int_peak** = Not Run

### Base Optimization Flags

**C benchmarks:**
- `-Wl,-z,muldefs` 
- `-xCORE-AVX512` 
- `-ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64`
- `-lqkmalloc`

**C++ benchmarks:**
- `-Wl,-z,muldefs` 
- `-xCORE-AVX512` 
- `-ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64`
- `-lqkmalloc`

**Fortran benchmarks:**
- `-Wl,-z,muldefs` 
- `-xCORE-AVX512` 
- `-ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs -align array32byte`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64`
- `-lqkmalloc`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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