## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**

Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

<table>
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<tr>
<th>SPECspeed®2017_int_base = 8.57</th>
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<tr>
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### Hardware

- **CPU Name:** Intel Xeon Silver 4215
- **Max MHz:** 3500
- **Nominal:** 2500
- **Enabled:** 16 cores, 2 chips
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 11 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 400 GB SATA SSD
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.2.193 released Dec-2018
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --

### Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base (8.57)</th>
</tr>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>16</td>
<td>5.90</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>16</td>
<td>8.42</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>16</td>
<td>11.5</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>16</td>
<td>5.37</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>16</td>
<td>11.3</td>
</tr>
<tr>
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<td>16</td>
<td>12.4</td>
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<td>16</td>
<td>4.99</td>
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<tr>
<td>641.leela_s</td>
<td>16</td>
<td>4.29</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>16</td>
<td>12.7</td>
</tr>
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<td>657.xz_s</td>
<td>16</td>
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### Results Table

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<th>Ratio</th>
<th>Seconds</th>
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</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>16</td>
<td>300</td>
<td>5.91</td>
<td>301</td>
<td>5.90</td>
<td>301</td>
<td>5.90</td>
<td>602.gcc_s</td>
<td>16</td>
<td>473</td>
<td>8.42</td>
<td>473</td>
<td>8.41</td>
<td>473</td>
<td>8.42</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>16</td>
<td>410</td>
<td>11.5</td>
<td>410</td>
<td>11.5</td>
<td>409</td>
<td>11.6</td>
<td>607.omnetpp_s</td>
<td>16</td>
<td>301</td>
<td>5.41</td>
<td>304</td>
<td>5.37</td>
<td>304</td>
<td>5.36</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>16</td>
<td>125</td>
<td>11.3</td>
<td>127</td>
<td>11.2</td>
<td>126</td>
<td>11.3</td>
<td>625.x264_s</td>
<td>16</td>
<td>142</td>
<td>12.4</td>
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<td>397</td>
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</tr>
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<td>657.xz_s</td>
<td>16</td>
<td>339</td>
<td>18.2</td>
<td>339</td>
<td>18.2</td>
<td>341</td>
<td>18.1</td>
</tr>
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**Operating System Notes**

Stack size set to unlimited using "ulimit –s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:
- `KMP_AFFINITY = "granularity=fine,scatter"
- `LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
- `OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

- memory using Redhat Enterprise Linux 7.5
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  - `sync; echo 3> /proc/sys/vm/drop_caches`

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

- built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcd88f2999c33d61f64985e45859ea9
running on linux-jimm Mon Apr 29 00:34:43 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
Stepping: 6
CPU MHz: 2500.000
CPU max MHz: 3500.0000
CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K

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Platform Notes (Continued)

L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
Flags: fpu vme de pse tsc msr pae mca cmov apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constants tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdqc fma cx16 xtrm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
issue_limit_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 invpcid_single intel_puin mba tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves csm cqm_pmap cqm_occu_pmap cqm_mbm_total cqm_mbm_local
lpbp ibrs ibrms stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospital avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7
  node 0 size: 385610 MB
  node 0 free: 384394 MB
  node 1 cpus: 8 9 10 11 12 13 14 15
  node 1 size: 387058 MB
  node 1 free: 382989 MB
  node distances:
    node 0 1
      0: 10 21
      1: 21 10

From /proc/meminfo
  MemTotal: 791212920 kB
  HugePages_Total: 0
  Hugepagesize: 4096 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"

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### Platform Notes (Continued)

```plaintext
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```plaintext
uname -a:
   Linux linux-jimm 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

```plaintext
run-level 3 Apr 28 21:48
```

```plaintext
SPEC is set to: /home/cpu2017
```

### Compiler Version Notes

```
C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
| 625.x264_s(base) 657.xz_s(base)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

```
C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
| 641.leela_s(base)
```

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Compiler Version Notes (Continued)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation
C benchmarks:
icc -m64 -std=c11
C++ benchmarks:
icpc -m64
Fortran benchmarks:
ifort -m64

Base Portability Flags
600.perlbmk_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

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#### Base Optimization Flags (Continued)

- **C benchmarks (continued):**
  - `-qopt-mem-layout-trans=4` - `qopenmp` - `DSPEC_OPENMP`
  - `-L/usr/local/je5.0.1-64/lib -ljemalloc`

- **C++ benchmarks:**
  - `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
  - `-qopt-mem-layout-trans=4`
  - `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64 -lqkmalloc`

- **Fortran benchmarks:**
  - `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4`
  - `-nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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