Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECspeed2017_fp_base = 77.2
SPECspeed2017_fp_peak = 77.5

CPU2017 License: 9019
Test Date: Apr-2019
Test Sponsor: Cisco Systems
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: Nov-2018

| Threads | 0 | 15.0 | 30.0 | 45.0 | 60.0 | 75.0 | 90.0 | 105 | 120 | 135 | 150 | 165 | 180 | 195 | 210 | 225 | 240 | 255 | 270 | 285 | 300 | 315 | 330 | 340 |
|---------|---|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 603.bwaves_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 607.cactuBSSN_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 619.lbm_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 621.wrf_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 627.cam4_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 628.pop2_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 638.imagick_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 644.nab_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 649.fotonik3d_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 654.roms_s | 16 |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

--- SPECspeed2017_fp_base (77.2)
--- SPECspeed2017_fp_peak (77.5)

Hardware
CPU Name: Intel Xeon Silver 4215
Max MHz.: 3500
Nominal: 2500
Enabled: 16 cores, 2 chips
Orderable: 1.2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 11 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
Storage: 1 x 400 GB SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
4.12.14-23-default
Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux;
Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux
Parallel: Yes
Firmware: Version 4.0.2.193 released Dec-2018
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Results Table

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<tr>
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<th>Ratio</th>
<th>Seconds</th>
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<td>77.0</td>
<td>205</td>
<td>76.9</td>
<td>205</td>
<td>76.8</td>
</tr>
</tbody>
</table>

SPECspeed2017_fp_base = 77.2
SPECspeed2017_fp_peak = 77.5

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
 sync; echo 3 > /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPEC CPU2017 Floating Point Speed Result

SPECspeed2017_fp_base = 77.2
SPECspeed2017_fp_peak = 77.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Apr-2019
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: Nov-2018

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bced8f2999c33d61f64985e45859ea9
running on linux-jimm Mon Apr 29 03:14:48 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
   model name : Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
       2 "physical id"s (chips)
       16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
   cpu cores : 8
   siblings : 8
   physical 0: cores 0 1 2 3 4 5 6 7
   physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
   Architecture: x86_64
   CPU op-mode(s): 32-bit, 64-bit
   Byte Order: Little Endian
   CPU(s): 16
   On-line CPU(s) list: 0-15
   Thread(s) per core: 1
   Core(s) per socket: 8
   Socket(s): 2
   NUMA node(s): 2
   Vendor ID: GenuineIntel
   CPU family: 6
   Model: 85
   Model name: Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
   Stepping: 6
   CPU MHz: 2500.000
   CPU max MHz: 3500.0000
   CPU min MHz: 1000.0000
   BogoMIPS: 5000.00
   Virtualization: VT-x
   L1d cache: 32K
   L1i cache: 32K
   L2 cache: 1024K
   L3 cache: 11264K

(Continued on next page)
SPEC CPU2017 Floating Point Speed Result

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECspeed2017_fp_base = 77.2
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Apr-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Platform Notes (Continued)

NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdscn
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
spec_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_ppin mba tpr_shadow vmmi flexpriority ept
vpid fsgsb Tear tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cmp mx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsave xsavec xgetbv1 xsave tcm cqm llc cqm_occup_llc cqm_mb_m_total cqm_mb_m_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospk avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7
  node 0 size: 385610 MB
  node 0 free: 381820 MB
  node 1 cpus: 8 9 10 11 12 13 14 15
  node 1 size: 387058 MB
  node 1 free: 385448 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 791212920 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

<table>
<thead>
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<td>Software Availability: Nov-2018</td>
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**SPEC CPU2017 Floating Point Speed Result**

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<th>SPECspeed2017_fp_base = 77.2</th>
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</thead>
<tbody>
<tr>
<td>SPECspeed2017_fp_peak = 77.5</td>
</tr>
</tbody>
</table>

---

**Platform Notes (Continued)**

```
uname -a:
    Linux linux-jimm 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Apr 28 21:48

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 btrfs 370G 9.7G 359G 3% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**BIOS** Cisco Systems, Inc. C220M5.4.0.2.193.1203182037 12/03/2018

**Memory:**

24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

---

**Compiler Version Notes**

```
==============================================================================
CC  619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base, peak)
-------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------------
```

```
FC  607.cactuBSSN_s(base, peak)
-------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
```

---

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

**Compiler Version Notes (Continued)**

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel (R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
   64, Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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<th>fotonik3d_s(base)</th>
<th>roms_s(base, peak)</th>
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<table>
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<th>fotonik3d_s(peak)</th>
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<th>cam4_s(base, peak)</th>
<th>pop2_s(base)</th>
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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz) SPECspeed2017_fp_base = 77.2 SPECspeed2017_fp_peak = 77.5

CPU2017 License: 9019 Test Date: Apr-2019
Test Sponsor: Cisco Systems Hardware Availability: Apr-2019
Tested by: Cisco Systems Software Availability: Nov-2018

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
                        -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECspeed2017_fp_base = 77.2
SPECspeed2017_fp_peak = 77.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test by: Cisco Systems

---

**Base Optimization Flags (Continued)**

Benchmarks using Fortran, C, and C++:
- `-xCORE-AVX512` `-ipo` `-O3` `-no-prec-div` `-qopt-prefetch`
- `-ffinite-math-only` `-qopt-mem-layout-trans=4` `-qopenmp` `-DSPEC_OPENMP`
- `-nostandard-realloc-lhs`

---

**Peak Compiler Invocation**

C benchmarks:
`icc -m64 -std=c11`

Fortran benchmarks:
`ifort -m64`

Benchmarks using both Fortran and C:
`ifort -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
`icpc -m64 icc -m64 -std=c11 ifort -m64`

---

**Peak Portability Flags**

Same as Base Portability Flags

---

**Peak Optimization Flags**

C benchmarks:
- `-xCORE-AVX512` `-ipo` `-O3` `-no-prec-div` `-qopt-prefetch`
- `-ffinite-math-only` `-qopt-mem-layout-trans=4` `-qopenmp` `-DSPEC_OPENMP`

Fortran benchmarks:

603.bwaves_s: `-prof-gen(pass 1)` `-prof-use(pass 2)` `-DSPEC_SUPPRESS_OPENMP` `-DSPEC_OPENMP -O2` `-xCORE-AVX512` `-qopt-prefetch` `-ipo` `-O3` `-ffinite-math-only` `-no-prec-div` `-qopt-mem-layout-trans=4` `-qopenmp` `-nostandard-realloc-lhs`

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: `-DSPEC_OPENMP` `-xCORE-AVX512` `-ipo` `-O3` `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only` `-qopt-mem-layout-trans=4`

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECspeed2017_fp_base = 77.2
SPECspeed2017_fp_peak = 77.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Peak Optimization Flags (Continued)

654.roms_s (continued):
   -qopenmp  -nostandard-realloc-lhs

Benchmarks using both Fortran and C:

621.wrf_s:  -prof-gen(pass 1)  -prof-use(pass 2)  -O2  -xCORE-AVX512
   -qopt-prefetch -ipo -O3  -ffinite-math-only  -no-prec-div
   -qopt-mem-layout-trans=4  -DSPEC_SUPPRESS_OPENMP  -qopenmp
   -DSPEC_OPENMP  -nostandard-realloc-lhs

627.cam4_s:  -xCORE-AVX512  -ipo -O3  -no-prec-div  -qopt-prefetch
   -ffinite-math-only  -qopt-mem-layout-trans=4  -qopenmp
   -DSPEC_OPENMP  -nostandard-realloc-lhs

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:

   -xCORE-AVX512  -ipo -O3  -no-prec-div  -qopt-prefetch
   -ffinite-math-only  -qopt-mem-layout-trans=4  -qopenmp  -DSPEC_OPENMP
   -nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

   http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revI.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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