## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS C240 M5 (Intel Xeon Silver 4216, 2.10GHz)

<table>
<thead>
<tr>
<th>Specrate®2017_int_base = 176</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specrate®2017_int_peak = Not Run</td>
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</table>

### CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Apr-2019  
Hardware Availability: Apr-2019  
Software Availability: Nov-2018

| Copies | 0 | 15.0 | 30.0 | 45.0 | 60.0 | 75.0 | 90.0 | 105 | 120 | 135 | 150 | 165 | 180 | 195 | 210 | 225 | 240 | 255 | 270 | 285 | 300 | 315 | 330 | 340 |
|--------|---|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 500.perlbench_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 502.gcc_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 505.mcf_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 520.omnetpp_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 523.xalancbmk_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 525.x264_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 531.deepsjeng_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 541.leela_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 548.exchange2_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 557.xz_r | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Hardware**

- **CPU Name:** Intel Xeon Silver 4216  
- **Max MHz:** 3200  
- **Nominal:** 2100  
- **Enabled:** 32 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 chips  
- **Cache L1:** 32 KB I+ 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 22 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)  
- **Storage:** 1 x 240 GB M.2 SATA SSD  
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++  
  Compiler Build 20181018 for Linux;  
  Fortran: Version 19.0.1.144 of Intel Fortran  
  Compiler Build 20181018 for Linux  
- **Parallel:** No  
- **Compiler Build:** 20181018 for Linux  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** None  
- **Power Management:** --
## Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4216, 2.10GHz)

### SPEC CPU®2017 Integer Rate Result

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<th>Benchmark</th>
<th>Copies</th>
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<th>Ratio</th>
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<tbody>
<tr>
<td>Base</td>
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<td>756</td>
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<td>150</td>
<td>608</td>
<td>149</td>
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<td>505.mcf_r</td>
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<td>121</td>
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<td>523.xalanbmk_r</td>
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<td>203</td>
<td>333</td>
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<td>332</td>
<td>204</td>
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<td>338</td>
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<td>146</td>
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<tr>
<td>541.leela_r</td>
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<td>64</td>
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<td>119</td>
<td>579</td>
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**Results Table**

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<td></td>
<td></td>
<td></td>
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</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

Memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4216, 2.10GHz)

<table>
<thead>
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<td>176</td>
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<td>Not Run</td>
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**General Notes (Continued)**
is mitigated in the system as tested and documented.

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-8ofr Fri Apr 26 22:46:59 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 16
  siblings : 32
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
```

(Continued on next page)
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| SPECrate®2017_int_base = 176 |
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Tested by: Cisco Systems

Platform Notes (Continued)

- CPU max MHz: 3200.0000
- CPU min MHz: 800.0000
- BogoMIPS: 4200.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 22528K
- NUMA node0 CPU(s): 0-3,8-11,32-35,40-43
- NUMA node1 CPU(s): 4-7,12-15,36-39,44-47
- NUMA node2 CPU(s): 16-19,24-27,48-51,56-59
- NUMA node3 CPU(s): 20-23,28-31,52-55,60-63
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nop1 xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtp cr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single mba tpr_shadow vmmi flexpriority ept vpid fsbgbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaev xsaveopt xsaves cqml1c cq_mpb_total cq_mpp_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp-epp hwp-pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data

- cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
- available: 4 nodes (0-3)
- node 0 cpus: 0 1 2 3 8 9 10 11 12 13 14 15 36 37 38 39 44 45 46 47
- node 0 size: 192103 MB
- node 0 free: 191788 MB
- node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
- node 1 size: 193527 MB
- node 1 free: 193303 MB
- node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
- node 2 size: 193498 MB
- node 2 free: 193012 MB
- node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
- node 3 size: 193526 MB
- node 3 free: 193262 MB
- node distances:
  - node 0 1 2 3
  - 0: 10 11 21 21
  - 1: 11 10 21 21

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Platform Notes (Continued)

2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
MemTotal:       791199892 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release*/etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-8ofr 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Apr 26 22:44

SPEC is set to: /home/cpu2017
Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda3      btrfs  222G  50G  172G  23% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. C240M5.4.0.3.34.0301190218 03/01/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)
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Compiler Version Notes
==============================================================================
| C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) |
|   | 525.x264_r(base) 557.xz_r(base)                  |
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
C++ | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) |
|    | 541.leela_r(base)                                           |
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
Fortran | 548.exchange2_r(base)                                      |
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64

(Continued on next page)
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SPECrates

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Base Portability Flags (Continued)

523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl, -z, multidefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl, -z, multidefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl, -z, multidefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revI.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-04-27 01:46:59-0400.
Report generated on 2020-08-04 20:01:27 by CPU2017 PDF formatter v6255.