Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4216, 2.10GHz)

SPECspeed2017_int_base = 8.41
SPECspeed2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
- CPU Name: Intel Xeon Silver 4216
- Max MHz.: 3200
- Nominal: 2100
- Enabled: 32 cores, 2 chips
- Orderable: 1.2 chips
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 22 MB I+D on chip per chip
- Other: None
- Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- Storage: 1 x 240 GB M.2 SATA SSD
- Other: None

Software
- OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux;
- Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux
- Parallel: Yes
- Firmware: Version 4.0.3.34 released Mar-2019
- File System: btrfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: Not Applicable
- Other: jemalloc memory allocator V5.0.1

Threads
- 600.perlbench_s 32
- 602.gcc_s 32
- 605.mcf_s 32
- 620.omnetpp_s 32
- 623.xalancbmk_s 32
- 625.x264_s 32
- 631.deepsjeng_s 32
- 641.leea_s 32
- 648.exchange2_s 32
- 657.xz_s 32

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018
Cisco Systems
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Base</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
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<td>631.deepsjeng_s</td>
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<tr>
<td>648.exchange2_s</td>
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<tr>
<td>657.xz_s</td>
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</tbody>
</table>

SPECspeed2017_int_base = 8.41
SPECspeed2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32;/home/cpu2017/lib/intel64;/home/cpu2017/je5.0.1-32;/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
 sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
SPEC CPU2017 Integer Speed Result

Cisco Systems
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Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcd8f2999c33d61f64985e45859ea9
running on linux-8ofr Mon Apr 29 03:37:37 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
Online CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4216, 2.10GHz)

SPECspeak2017_int_base = 8.41
SPECspeak2017_int_peak = Not Run

L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpre pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ersedm invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occcll cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/cache/data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

Available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385634 MB
node 0 free: 384903 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387027 MB
node 1 free: 382552 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 791206376 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4216, 2.10GHz)

**SPEC CPU2017 Integer Speed Result**

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**CPU2017 License:** 9019  
**Test Date:** Apr-2019

**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Apr-2019

**Tested by:** Cisco Systems  
**Software Availability:** Nov-2018

**Platform Notes (Continued)**

```plaintext
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```plaintext
uname -a:
Linux linux-8ofr 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

```
run-level 3 Apr 29 00:51
```

**SPEC is set to:** /home/cpu2017

```
Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sda3      btrfs  222G   53G  169G  24% /home
```

Additional information from dmidecode follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- BIOS Cisco Systems, Inc. C240M5.4.0.3.34.0301190218 03/01/2019
- Memory: 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

*(End of data from sysinfo program)*

**Compiler Version Notes**

```
(Continued on next page)
```
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4216, 2.10GHz)

SPEC CPU2017 Integer Speed Result

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

FC 648.exchange2_s(base)
------------------------------------------------------------------------------

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

(Continued on next page)
## SPEC CPU2017 Integer Speed Result

### Cisco Systems

**Cisco UCS C240 M5 (Intel Xeon Silver 4216, 2.10GHz)**

<table>
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<tr>
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<th>Value</th>
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<tr>
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**Software Availability:** Nov-2018

### Base Optimization Flags (Continued)

- **C benchmarks (continued):**
  - `qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`
  - `-L/usr/local/je5.0.1-64/lib -ljemalloc`

- **C++ benchmarks:**
  - `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
  - `qopt-mem-layout-trans=4`
  - `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64 -lqkmalloc`

- **Fortran benchmarks:**
  - `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4`
  - `nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-04-29 06:37:36-0400.