## SPEC® CPU2017 Integer Rate Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
**ProLiant ML350 Gen10**  
(2.50 GHz, Intel Xeon Gold 5215L)

### Software

<table>
<thead>
<tr>
<th>SPECrate2017_int_base</th>
<th>Specrate2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>119</td>
<td>Not Run</td>
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</table>

<table>
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<tr>
<th>SPECrate2017_int_base = 119</th>
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**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE  
**Hardware Availability:** Apr-2019  
**Software Availability:** Feb-2019  
**Test Date:** May-2019

<table>
<thead>
<tr>
<th>SPECrate2017_int_base (119)</th>
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</table>

### Hardware

**CPU Name:** Intel Xeon Gold 5215L  
**Max MHz.:** 3400  
**Nominal:** 2500  
**Enabled:** 20 cores, 2 chips, 2 threads/core  
**Orderable:** 1, 2 chip(s)  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 13.75 MB I+D on chip per chip  
**Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R, running at 2666)  
**Storage:** 1 x 400 GB SAS SSD, RAID 0  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 15 (x86_64)  
**Kernel:** 4.12.14-23-default  
**Compiler:** C/C++: Version 19.0.2.187 of Intel C/C++ Compiler Build 20190117 for Linux; Fortran: Version 19.0.2.187 of Intel Fortran Compiler Build 20190117 for Linux  
**Parallel:** No  
**Firmware:** HPE BIOS Version U41 02/02/2019 released Apr-2019  
**File System:** btrfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** Not Applicable  
**Other:** None

### Copies

<table>
<thead>
<tr>
<th>Test</th>
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<th>Result</th>
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<tbody>
<tr>
<td>500.perbench_r</td>
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<td>98.8</td>
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<tr>
<td>502.gcc_r</td>
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<td>161</td>
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<tr>
<td>505.mcf_r</td>
<td>40</td>
<td>80.4</td>
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<tr>
<td>520.omnetpp_r</td>
<td>40</td>
<td>135</td>
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<tr>
<td>523.xalancbmk_r</td>
<td>40</td>
<td>235</td>
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<tr>
<td>525.x264_r</td>
<td>40</td>
<td>210</td>
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<tr>
<td>531.deepsjeng_r</td>
<td>40</td>
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<td>541.leela_r</td>
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<tr>
<td>548.exchange2_r</td>
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<tr>
<td>557.xz_r</td>
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### Results Table

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</tbody>
</table>

**SPECrate2017_int_base =** 119  
**SPECrate2017_int_peak =** Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The `numactl` mechanism was used to bind copies to processors. The config file option 'submit' was used to generate `numactl` commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
```
    sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:  
```
    numactl --interleave=all runcpu <etc>
```

### General Notes

Environment variables set by runcpu before the start of the run:  
```
    LD_LIBRARY_PATH = "/home/cpu2017_u2/lib/ia32/:/home/cpu2017_u2/lib/intel64"
```

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5  
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
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Hewlett Packard Enterprise
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CPU2017 License: 3
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Tested by: HPE

SPECrate2017_int_base = 119
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Test Date: May-2019
Hardware Availability: Apr-2019
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General Notes (Continued)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017_u2/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on ml350-sles15 Wed May  1 01:21:11 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 5215L CPU @ 2.50GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5215L CPU @ 2.50GHz

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Platform Notes (Continued)

Stepping: 6
CPU MHz: 2500.000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperp tsc_known_freq pni pclmulqdq dtst64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcld dca sse4_1 sse4_2 x2apic movbe popcnt
	tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cd8_l3 invpcid_single intel_pmm mba tpr_shadow vnumi flexpriority ept
vpid fsgsbase tsc_adjust bmi hle avx2 mmp bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap cflusshopt clwb intel_pt avx512cd avx512bw avx512vl
xsaeveopt xsavec xgetbv1 xsavees cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pin pts pkun ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data

(cache size: 14080 KB)

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
node 0 size: 193089 MB
node 0 free: 192596 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
node 1 size: 193531 MB
node 1 free: 193243 MB

node distances:
node 0 1
0: 21
1: 21

From /proc/meminfo

MemTotal: 395899944 KB
HugePages_Total: 0
Hugepagesize: 2048 KB

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"

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Platform Notes (Continued)

VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux ml350-sles15 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 May 1 01:17

SPEC is set to: /home/cpu2017_u2

Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sdb2      btrfs  371G  211G  159G  57% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS HPE U41 02/02/2019
Memory:
    24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base)
     557.xz_r(base)
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
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- **Test Date:** May-2019
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**Compiler Version Notes (Continued)**

```plaintext
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) 541.leela_r(base)
```

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```plaintext
FC 548.exchange2_r(base)
```

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

**Base Compiler Invocation**

C benchmarks:  
```plaintext
icc -m64 -std=c11
```

C++ benchmarks:  
```plaintext
icpc -m64
```

Fortran benchmarks:  
```plaintext
ifort -m64
```

**Base Portability Flags**

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalanchbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64
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**Base Optimization Flags**

C benchmarks:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64 -lqkmalloc`

C++ benchmarks:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64 -lqkmalloc`

Fortran benchmarks:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64 -lqkmalloc`

The flags files that were used to format this result can be browsed at:
- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.html](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.html)  

You can also download the XML flags sources by saving the following links:
- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.xml](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.xml)  

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-04-30 15:51:11-0400.  
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