## SPEC® CPU2017 Integer Rate Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
ProLiant ML110 Gen10  
(2.50 GHz, Intel Xeon Silver 4215)  

<table>
<thead>
<tr>
<th>SPECrate2017_int_base =</th>
<th>49.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_int_peak =</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

### CPU2017 License: 3  
Test Sponsor: HPE  
Tested by: HPE  
Test Date: Apr-2019  
Hardware Availability: Apr-2019  
Software Availability: Feb-2019

### Hardware

- **CPU Name:** Intel Xeon Silver 4215  
- **Max MHz.:** 3500  
- **Nominal:** 2500  
- **Enabled:** 8 cores, 1 chip, 2 threads/core  
- **Orderable:** 1 chip(s)  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 11 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 96 GB (6 x 16 GB 2Rx8 PC4-2666V-R, running at 2400)  
- **Storage:** 1 x 400 GB SAS SSD, RAID 0  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
- **Kernel:** 4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.2.187 of Intel C/C++ Compiler Build 20190117 for Linux; Fortran: Version 19.0.2.187 of Intel Fortran Compiler Build 20190117 for Linux  
- **Parallel:** No  
- **Firmware:** HPE BIOS Version U33 02/02/2019 released Apr-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** None

### SPECrate2017_int_base (49.2)
SPEC CPU2017 Integer Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant ML110 Gen10
(2.50 GHz, Intel Xeon Silver 4215)

SPECrate2017_int_base = 49.2
SPECrate2017_int_peak = Not Run

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>16</td>
<td>686</td>
<td>37.1</td>
<td>687</td>
<td>37.1</td>
<td>686</td>
<td>37.1</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>16</td>
<td>537</td>
<td>42.2</td>
<td>536</td>
<td>42.3</td>
<td>536</td>
<td>42.3</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>16</td>
<td>383</td>
<td>67.6</td>
<td>383</td>
<td>67.5</td>
<td>383</td>
<td>67.5</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>16</td>
<td>627</td>
<td>33.5</td>
<td>629</td>
<td>33.4</td>
<td>629</td>
<td>33.4</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>16</td>
<td>282</td>
<td>59.9</td>
<td>283</td>
<td>59.8</td>
<td>283</td>
<td>59.7</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>16</td>
<td>296</td>
<td>94.6</td>
<td>297</td>
<td>94.4</td>
<td>296</td>
<td>94.5</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>16</td>
<td>450</td>
<td>40.7</td>
<td>450</td>
<td>40.7</td>
<td>450</td>
<td>40.7</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>16</td>
<td>719</td>
<td>36.9</td>
<td>719</td>
<td>36.9</td>
<td>719</td>
<td>36.8</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>16</td>
<td>489</td>
<td>85.7</td>
<td>489</td>
<td>85.7</td>
<td>489</td>
<td>85.8</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>16</td>
<td>541</td>
<td>31.9</td>
<td>540</td>
<td>32.0</td>
<td>540</td>
<td>32.0</td>
</tr>
</tbody>
</table>

SPECrate2017_int_base = 49.2
SPECrate2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
  numactl --interleave=all runcpu <etc>

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017_u2/lib/ia32;/home/cpu2017_u2/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9–7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
SPEC CPU2017 Integer Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant ML110 Gen10
(2.50 GHz, Intel Xeon Silver 4215)

SPECrate2017_int_base = 49.2
SPECrate2017_int_peak = Not Run

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

General Notes (Continued)

is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance
Sysinfo program /home/cpu2017_u2/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on ml110-sles15 Mon Apr 29 22:43:15 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
  1 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7

From lscpu:

Architecture:  x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 1
NUMA node(s): 1
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
Stepping: 6
CPU MHz: 2500.000

(Continued on next page)
System: Hewlett Packard Enterprise
CPU: ProLiant ML110 Gen10 (2.50 GHz, Intel Xeon Silver 4215)
Test Sponsor: HPE
Software Availability: Feb-2019
Hardware Availability: Apr-2019
Test Date: Apr-2019

SPEC CPU2017 Integer Rate Result

SPECrate2017_int_base = 49.2
SPECrate2017_int_peak = Not Run

CPU2017 License: 3

Platform Notes (Continued)

BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-15
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdg_l3 invpcid_single intel_pinn mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmel hle avx2 smep bmi2 erms invpcid rtm cqm avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsavec cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs stibp dtherm ida arat pin pts pku ospke avx512_vnni arch_capabilities ssbd

From /proc/cpuinfo cache data
  cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 1 nodes (0)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  node 0 size: 96324 MB
  node 0 free: 95808 MB
  node distances:
    node 0
  0: 10

From /proc/meminfo
  MemTotal: 98636204 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

(Continued on next page)
Platform Notes (Continued)

uname -a:
    Linux ml110-sles15 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Apr 29 22:40

SPEC is set to: /home/cpu2017_u2
    Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda3      xfs   313G   39G  274G  13% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS HPE U33 02/02/2019
    Memory:
        6x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
  CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base)
  557.xz_r(base)
  Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.2.187 Build 20190117
  Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
  CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
  541.leela_r(base)
  Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.2.187 Build 20190117
  Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant ML110 Gen10
(2.50 GHz, Intel Xeon Silver 4215)

SPEC CPU2017 Integer Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

<table>
<thead>
<tr>
<th>CPU2017 License: 3</th>
<th>Test Date: Apr-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: HPE</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: HPE</td>
<td>Software Availability: Feb-2019</td>
</tr>
</tbody>
</table>

SPECrate2017_int_base = 49.2
SPECrate2017_int_peak = Not Run

Compiler Version Notes (Continued)
------------------------------------------------------------------------------
FC 548.exchange2_r(base)
------------------------------------------------------------------------------

Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

(Continued on next page)
Hewlett Packard Enterprise (Test Sponsor: HPE)
ProLiant ML110 Gen10 (2.50 GHz, Intel Xeon Silver 4215)

SPECrate2017_int_base = 49.2
SPECrate2017_int_peak = Not Run

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE
Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

Base Optimization Flags (Continued)

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.xml
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2019-04-03.xml

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-04-29 13:13:14-0400.
Originally published on 2019-06-11.