Dell Inc. PowerEdge FC640 (Intel Xeon Silver 4215, 2.50GHz)

<table>
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<tr>
<th>SPECrate2017_fp_base</th>
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CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.
Test Date: Mar-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

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<tr>
<td>510.parest_r 16</td>
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<td>526.blender_r 16</td>
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<tr>
<td>554.roms_r 16</td>
<td>64.1</td>
</tr>
</tbody>
</table>

Hardware

- CPU Name: Intel Xeon Silver 4215
- Max MHz.: 3500
- Nominal: 2500
- Enabled: 16 cores, 2 chips
- Orderable: 1.2 chips
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 11 MB I+D on chip per chip
- Other: None
- Memory: 384 GB (12 x 32 GB 2Rx8 PC4-2933Y-R, running at 2400)
- Storage: 1 x 480 GB SATA SSD
- Other: None

Software

- OS: Ubuntu 18.04.2 LTS
- Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux;
- Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux
- Parallel: No
- Firmware: Version 2.2.2 released Mar-2019
- File System: ext4
- System State: Run level 5 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: 64-bit
- Other: None
Dell Inc.

PowerEdge FC640 (Intel Xeon Silver 4215, 2.50GHz)

Results Table

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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default.
Prior to runcpu invocation

(Continued on next page)
### SPEC CPU2017 Floating Point Rate Result

#### Dell Inc.

**PowerEdge FC640 (Intel Xeon Silver 4215, 2.50GHz)**

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**SPECrate2017_fp_base = 100**

**SPECrate2017_fp_peak = 103**

### General Notes (Continued)

Filesystem page cache synced and cleared with:
```
sync; echo 3>/proc/sys/vm/drop_caches
```
runcpu command invoked through numactl i.e.:
```
numactl --interleave=all runcpu <etc>
```

### Platform Notes

- BIOS settings:
  - ADDDC setting disabled
  - Sub NUMA Cluster enabled
  - Virtualization Technology disabled
  - DCU Streamer Prefetcher enabled
  - System Profile set to Custom
  - CPU Performance set to Maximum Performance
  - C States set to Autonomous
  - C1E disabled
  - Uncore Frequency set to Dynamic
  - Energy Efficiency Policy set to Performance
  - Memory Patrol Scrub disabled
  - Logical Processor disabled
  - CPU Interconnect Bus Link Power Management disabled
  - PCI ASPM L1 Link Power Management disabled
  - Sysinfo program /home/cpu2017/bin/sysinfo
  - Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
    running on intel-sut Tue Apr 16 00:55:25 2019

SUT (System Under Test) info as seen by some common utilities. For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name: Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
  - 2 "physical id"s (chips)
  - 16 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores: 8
  - siblings: 8
  - physical 0: cores 0 1 2 3 4 5 6 7
  - physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:

- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 16

(Continued on next page)
## SPEC CPU2017 Floating Point Rate Result

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</tbody>
</table>

### Platform Notes (Continued)

On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
Stepping: 6
CPU MHz: 2160.191
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0,2,4,6,8,10,12,14
NUMA node1 CPU(s): 1,3,5,7,9,11,13,15

Flags: fpu vme de pse mcr msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperorf perfctr pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt aes xsave avx f16c rdrand
lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single ssbd mba ibrs
ibpb stibp ibrs_enhanced tpr_shadow vmi flexpriority ept vpid fsgsbase tsc_adjust
bmi1 hle avx2 smep bmi2 ets invpcid rtm cmqm mpx rdt_a avx512f avx512dq rdseed adx
smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1
xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts ksu
ospke avx512_vnni flush_lld arch_capabilities

```
/proc/cpuinfo cache data
cache size : 11264 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
  node 0 cpus: 0 2 4 6 8 10 12 14
  node 0 size: 191913 MB
  node 0 free: 191083 MB
  node 1 cpus: 1 3 5 7 9 11 13 15
  node 1 size: 193533 MB
  node 1 free: 192727 MB
node distances:
  node 0 1
    0: 10 21
    1: 21 10

(Continued on next page)
<table>
<thead>
<tr>
<th>Platform Notes (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>From /proc/meminfo</td>
</tr>
<tr>
<td>MemTotal: 394698548 kB</td>
</tr>
<tr>
<td>HugePages_Total: 0</td>
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<tr>
<td>Hugepagesize: 2048 kB</td>
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<tr>
<td>/usr/bin/lsb_release -d</td>
</tr>
<tr>
<td>Ubuntu 18.04.2 LTS</td>
</tr>
<tr>
<td>From /etc/<em>release</em></td>
</tr>
<tr>
<td>debian_version: buster/sid</td>
</tr>
<tr>
<td>os-release:</td>
</tr>
<tr>
<td>NAME=&quot;Ubuntu&quot;</td>
</tr>
<tr>
<td>VERSION=&quot;18.04.2 LTS (Bionic Beaver)&quot;</td>
</tr>
<tr>
<td>ID=ubuntu</td>
</tr>
<tr>
<td>ID_LIKE=debian</td>
</tr>
<tr>
<td>PRETTY_NAME=&quot;Ubuntu 18.04.2 LTS&quot;</td>
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<td>VERSION_ID=&quot;18.04&quot;</td>
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</table>
| HOME_URL="https://www.ubuntu.com/"
| SUPPORT_URL="https://help.ubuntu.com/"
| uname -a:               |
| Linux intel-sut 4.15.0-45-generic #48-Ubuntu SMP Tue Jan 29 16:28:13 UTC 2019 x86_64 x86_64 GNU/Linux |
| Kernel self-reported vulnerability status: |
| CVE-2017-5754 (Meltdown): Not affected |
| CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization |
| CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB |
| run-level 5 Apr 15 19:24 |
| SPEC is set to: /home/cpu2017 |
| Filesystem Type Size Used Avail Use% Mounted on |
| /dev/sda2 ext4 439G 19G 398G 5% / |
| Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard. |
| BIOS Dell Inc. 2.2.2 03/05/2019 |
| Memory: |
| 3x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2400 |
| 9x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2400 |
| 4x Not Specified Not Specified |
SPEC CPU2017 Floating Point Rate Result

Dell Inc.

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SPECrate2017_fp_base = 100

SPECrate2017_fp_peak = 103

Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

================================================================================
CC 519.lbm_r(base) 538.imagick_r(base, peak) 544.nab_r(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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**Compiler Version Notes (Continued)**

```
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Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
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Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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### Compiler Version Notes (Continued)

```plaintext
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
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Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

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C   521.wrf_r(peak) 527.cam4_r(peak)
```

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Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

### Base Compiler Invocation

**C benchmarks:**
```
icc -m64 -std=c11
```

**C++ benchmarks:**
```
icpc -m64
```

**Fortran benchmarks:**
```
ifort -m64
```

**Benchmarks using both Fortran and C:**
```
ifort -m64 icc -m64 -std=c11
```

**Benchmarks using both C and C++:**
```
icpc -m64 icc -m64 -std=c11
```

**Benchmarks using Fortran, C, and C++:**
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

### Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
```

(Continued on next page)
SPEC CPU2017 Floating Point Rate Result

Dell Inc.

PowerEdge FC640 (Intel Xeon Silver 4215, 2.50GHz)

SPECrates2017_fp_base = 100
SPECrates2017_fp_peak = 103

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.
Test Date: Mar-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

Base Portability Flags (Continued)

511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte
Dell Inc.
PowerEdge FC640 (Intel Xeon Silver 4215, 2.50GHz)

SPECrate2017_fp_base = 100
SPECrate2017_fp_peak = 103

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.
Test Date: Mar-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

(Continued on next page)
Peak Optimization Flags (Continued)

510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
**Dell Inc.**

**PowerEdge FC640 (Intel Xeon Silver 4215, 2.50GHz)**

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.