Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230, 2.10GHz)

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate2017_int_base = 226</th>
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<tbody>
<tr>
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<td>80</td>
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<td>80</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>80</td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Gold 6230
Max MHz.: 3900
Nominal: 2100
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 27.5 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++
Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran
Compiler for Linux
Parallel: No
Firmware: Version 4.0.4c released Apr-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
## Results Table

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</tr>
</tbody>
</table>

**SPECrate2017_int_base = 226**

**SPECrate2017_int_peak = 235**

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### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```
sync; echo 3 > /proc/sys/vm/drop_caches
```
runcpu command invoked through numactl i.e.:
```
umactl --interleave=all runcpu <etc>
```
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6230, 2.10GHz)

SPECrate2017_int_base = 226
SPECrate2017_int_peak = 235

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-4z0x Thu Jun 20 14:04:57 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6230 CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6230 CPU @ 2.10GHz
Stepping: 6

(Continued on next page)
Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6230, 2.10GHz)

Copyright 2017-2019 Standard Performance Evaluation Corporation

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Jun-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU MHz:</td>
<td>2100.000</td>
</tr>
<tr>
<td>CPU max MHz:</td>
<td>3900.000</td>
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<tr>
<td>CPU min MHz:</td>
<td>800.000</td>
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<tr>
<td>BogoMIPS:</td>
<td>4200.00</td>
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<td>Virtualization:</td>
<td>VT-x</td>
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<tr>
<td>L1i cache:</td>
<td>32K</td>
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<tr>
<td>L2 cache:</td>
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<tr>
<td>L3 cache:</td>
<td>28160K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59</td>
</tr>
<tr>
<td>NUMA node2 CPU(s):</td>
<td>20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
<td>23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

```
From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
  node 0 size: 192101 MB
  node 0 free: 191736 MB
  node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
  node 1 size: 193497 MB
  node 1 free: 193190 MB
  node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
  node 2 size: 193526 MB
  node 2 free: 193290 MB
  node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
  node 3 size: 193525 MB
  node 3 free: 193170 MB
  node distances:
    node 0 1 2 3
       0: 10 11 21 21
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230, 2.10GHz)

SPECrate2017_int_base = 226
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Platform Notes (Continued)

1:  11  10  21  21
2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
MemTotal:       791195876 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-4z0x 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Jun 20 14:00

SPEC is set to: /home/cpu2017
Filesystem  Type  Size  Used Avail Use% Mounted on
/dev/sda1    xfs  891G  31G  860G   4% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. C240M5.4.0.4c.0.0411190411 04/11/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230, 2.10GHz)

SPECrate2017_int_base = 226
SPECrate2017_int_peak = 235

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes

==============================================================================
CC   502.gcc_r(peak)
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
    525.x264_r(base, peak) 557.xz_r(base, peak)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
CC   500.perlbench_r(peak)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
CXXC 523.xalancbmk_r(peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
CXXC 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base,
    peak) 541.leetla_r(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
FC  548.exchange2_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230, 2.10GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Jun-2019
Hardware Availability: Apr-2019
Test Sponsor: Cisco Systems
Software Availability: May-2019
Tested by: Cisco Systems

Compiler Version Notes (Continued)
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc

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## SPEC CPU2017 Integer Rate Result

### Cisco Systems

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- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Test Date:** Jun-2019
- **Tested by:** Cisco Systems
- **Hardware Availability:** Apr-2019
- **Software Availability:** May-2019

### Base Optimization Flags (Continued)

For Fortran benchmarks:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

### Peak Compiler Invocation

**C benchmarks (except as noted below):**

```bash
icc -m64 -std=c11
```

```bash
```

**C++ benchmarks (except as noted below):**

```bash
icpc -m64
```

```bash
523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

For Fortran benchmarks:

```bash
ifort -m64
```

### Peak Portability Flags

- `500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `502.gcc_r: -D_FILE_OFFSET_BITS=64`
- `505.mcf_r: -DSPEC_LP64`
- `520.omnetpp_r: -DSPEC_LP64`
- `523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
- `525.x264_r: -DSPEC_LP64`
- `531.deepsjeng_r: -DSPEC_LP64`
- `541.leela_r: -DSPEC_LP64`
- `548.exchange2_r: -DSPEC_LP64`
- `557.xz_r: -DSPEC_LP64`

### Peak Optimization Flags

**C benchmarks:**

```bash
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
```

```bash
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
```

(Continued on next page)
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Cisco UCS C240 M5 (Intel Xeon Gold 6230, 2.10GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags (Continued)

500.perlbench_r (continued):
- fno-strict-overflow
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
- -xcORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
- -L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xcORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=4
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

525.x264_r: -Wl,-z,muldefs -xcORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=4 -fno-alias
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xcORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=4
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
- -xcORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
- -L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xcORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

The flags files that were used to format this result can be browsed at
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6230, 2.10GHz)

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<tr>
<td>SPECrate2017_int_peak</td>
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jun-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml